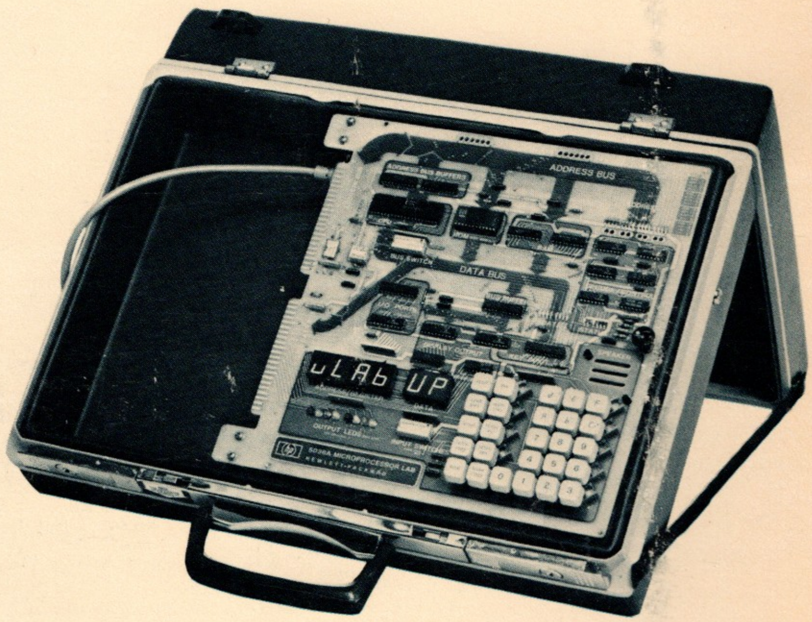
HP 5036A

SERVICE MANUAL

5036A
MICROPROCESSOR LAB



HEWLETT PACKARD

HP 5036A

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section I for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenace by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

5036A

MICROPROCESSOR LAB

SERVICE MANUAL

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed 1848.

MANUAL PART NO. 05036-90001
MICROFICHE PART NO. 05036-90002

Printed: FEBRUARY 1979

HEWLETT PACKARD

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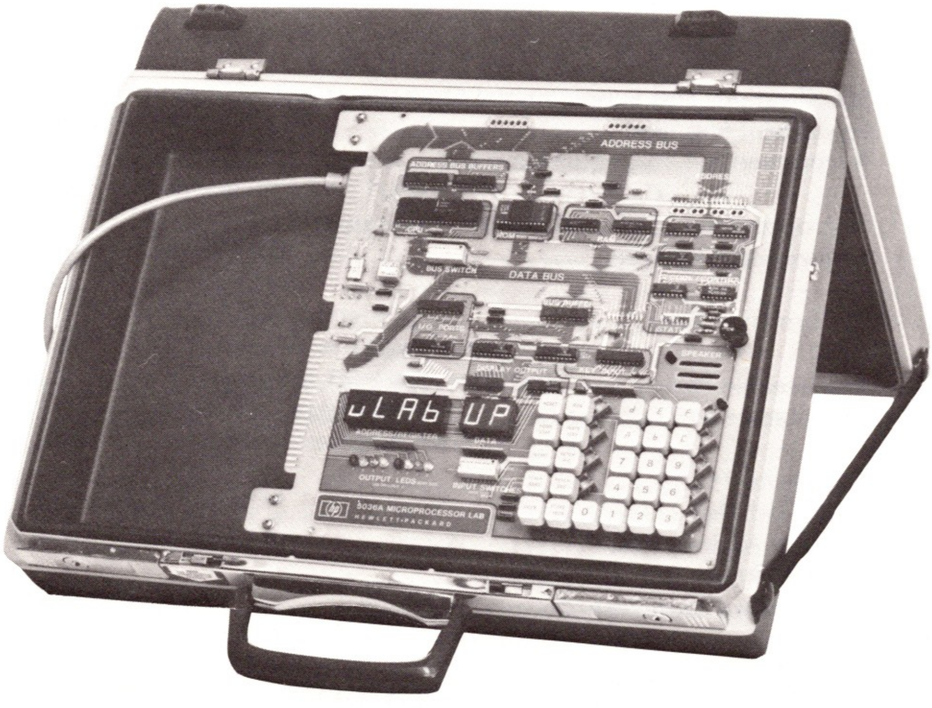


MODEL NO. 5036A

"PRACTICAL MICROPROCESSORS" TEXTBOOK
PART NO. 05036-90003

POWER CORD
PART NO. 8120-1378

Figure 1-1. HP 5036A Microprocessor Lab

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This service manual contains information needed to test and service the Hewlett-Packard Model 5036A Microprocessor Lab. *Figure 1-1* shows the 5036A.

1-3. SAFETY CONSIDERATIONS

1-4. The 5036A Microprocessor Lab is a Safety Class I instrument (provided with a protective earth terminal).

1-5. This service manual contains information, cautions, and warnings which must be followed by the user to ensure safe operation and keep the instrument in safe condition.

1-6. INSTRUMENTS COVERED BY MANUAL

1-7. Attached to the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-8. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-9. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-10. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-11. SPECIFICATIONS

1-12. Specifications and supplemental operating characteristics are listed in *Table 1-1*.

Table 1-1. Specifications and Supplemental Operating Characteristics

SPECIFICATIONS

Time Base Output: 2 MHz ±0.05%, crystal controlled

I/O Ports:
Output Drive: Each output will drive a minimum of one LS TTL load.
Input Loading: Each input equals no more than 3 LS TTL loads.

Power Supply:
Supply 1: 5V dc ±10%, >250 mA available for external circuitry.
Supply 2: 5V dc ±10%, >175 mA available for external circuitry.

Power Requirements: 100/120/220/240V ac ±10% 48 to 66 Hz line; 5VA maximum.

Dimensions: 514.4mm L × 371.5mm W × 177.8mm H (20.25 in. × 14.625 in. × 7.0 in.)

Weight: Shipping: 7.7 kg (17 lbs.)
Net: 6.73 kg (14 lbs. 10 oz.)

SUPPLEMENTAL OPERATING CHARACTERISTICS

Microprocessor: 8085A

ROM: 2316E; 2K Bytes

RAM: Two 2114/4045's; 1K Bytes

Displays:
Address/Register Display: 4 digits; 7-segment LED displays
Data Display: 2 digits; 7-segment LED displays
Output Port: 8 LED's; one per output line
Address Bus: 16 LED's; one per line
Data Bus: 8 LED's; one per line
Status Lines: 6 LED's; one per line

I/O: 8-bit latched output port with LED indicators.
8-bit input port with DIP switch.

Signature Analysis:
8-bit DIP switch used to disconnect MPU data lines from data bus.
"SA Loop" switch selects test loop program.
"Free-Run" switch selects free-run test mode.

Troubleshooting Jumpers:
12 user-programmable fault jumpers on circuit board simulate various hardware faults.

Troubleshooting Documentation:
Troubleshooting tree, block diagram, schematic, signature tables provided to determine faulty nodes.

1-13. DESCRIPTION

1-14. The 5036A Microprocessor Lab is a microcomputer designed for educational use, mounted in a briefcase. See *Figure 1-1.* The 5036A contains a keyboard for entering programs in machine code and a hexadecimal display for examining the memory. Operation is controlled by a special monitor program in ROM. This program scans the keyboard, sends data to the display and performs all control functions. Input switches and output LEDs are provided as peripherals. Indicator LEDs are installed in all address, data and control lines. Special switches are provided to establish loop operations for test purposes. Movable jumpers are included to insert faults in the circuits for training in troubleshooting microprocessor circuits.

1-15. EQUIPMENT SUPPLIED

1-16. *Table 1-2* lists equipment supplied.

Table 1-2. Equipment Supplied

Description	HP Part No.
Detachable Power Cord 231 cm (7.5 ft.) long	8120-1378
"Practical Microprocessors" Textbook	05036-90003

1-17. OPTIONS

1-18. Two options are available for the 5036A as listed below:

a. Option 001. Additional Copy of "Practical Microprocessors" textbook.

b. Option 910. Additional copy of Service Manual.

1-19. RECOMMENDED TEST EQUIPMENT

1-20. *Table 1-3* lists recommended test equipment to test, maintain, and troubleshoot the 5036A.

Table 1-3. Recommended Test Equipment

Instrument	Critical Specs	Recommended HP Model
Signature Analyzer	5036A compatibility	HP 5004A
Logic Probe	TTL compatibility	*HP 545A
Logic Pulser	TTL compatibility	*HP 546A
Logic Current Tracer	1 ma—1A Range	*HP 547A
Frequency Counter	10 Hz to 80 MHz	HP 5381A
Digital Voltmeter	10 volts	HP 3476A

**The HP 545A, 546A and 547A are available as a kit, Model 5024A.*

1-21. PERIPHERALS

1-22. Peripheral equipment may be connected to the 5036A as described in Appendix G of the "Practical Microprocessors" textbook. The 5036A is connected to peripheral equipment by means of two dual 22-pin edge connectors, HP Part No. 1251-2680 (Cinch 251-22-30-341).

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section provides information for inspection, installation, and preparation for use of the 5036A Microprocessor Lab.

2-3. INITIAL INSPECTION

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in *Figure 1-1*. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the 5036A does not pass the performance test, notify the nearet Hewlett-Packard office. If the shipping container is damaged, or the cushioning material show signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE

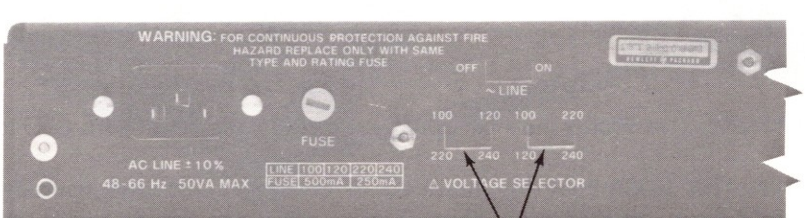
2-6. Line Voltage Requirements

CAUTION

BEFORE CONNECTING THE 5036A TO AC POWER LINES, BE SURE THAT THE VOLTAGE SELECTOR SWITCH IS PROPERLY POSITIONED AND THE CORRECT FUSE INSTALLED AS DESCRIBED BELOW.

2-7. The 5036A power supply is equipped with a VOLTAGE SELECTOR switch (below the LINE ON-OFF switch) to select 100-, 120-, 220-, or 240-volt operation. Before applying power, both VOLTAGE SELECTOR switches, shown in *Figure 2-1*, must be set to the voltage selector numbers that match the line voltage available.

2-8. The correct value line fuse, with a 250-volt rating must be installed in the fuseholder (adjacent to the switch). The 5036A uses a 0.5A fast-blo fuse (HP Part No. 2110-0012) for 100/120-volt operation and uses a 0.25A fast-blo fuse (HP Part No. 2110-0004) for 220/240-volt operation.



SLIDE BOTH SWITCHES
TO POSITION THAT MATCHES THE LINE VOLTAGE

Figure 2-1. Voltage Selector Switch

2-9. Power Cable

2-10. The 5036A is shipped with a three-wire power cable. When the cable is connected to an appropriate ac power source, this cable connects internal "grounds" in the 5036A to earth ground. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to *Figure 2-2* for the part numbers of the power cable and plug configurations available.

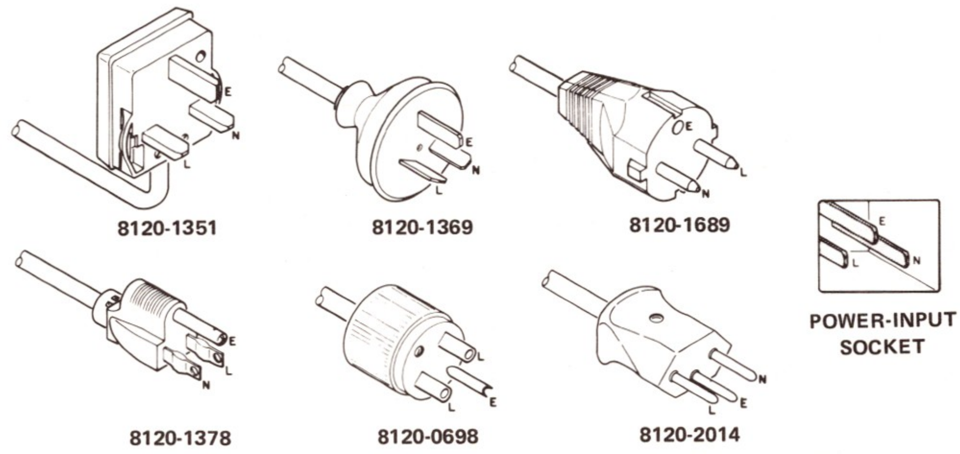


Figure 2-2. Power Cable HP Part Numbers Versus Mains Plugs Available

WARNING

BEFORE SWITCHING ON THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINALS MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

2-11. Operating Environment

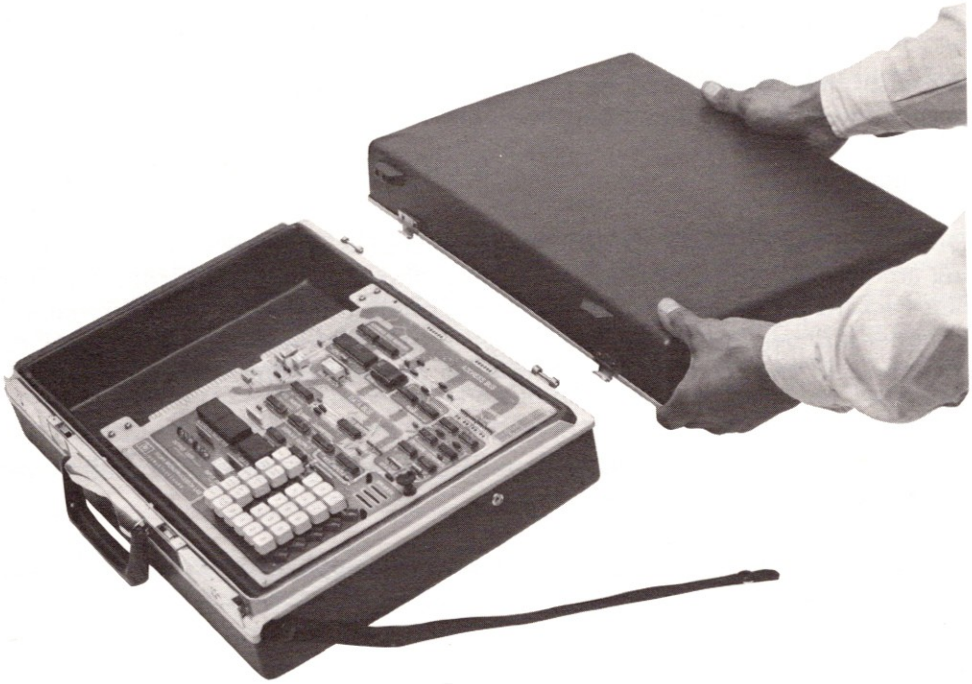
2-12. TEMPERATURE. The 5036A may be operated in temperatures from 0°C to +55°C.

2-13. HUMIDITY. The 5036A may be operated in environments with humidity up to 95%. However, it should be protected from temperature extremes which cause condensation in the instrument.

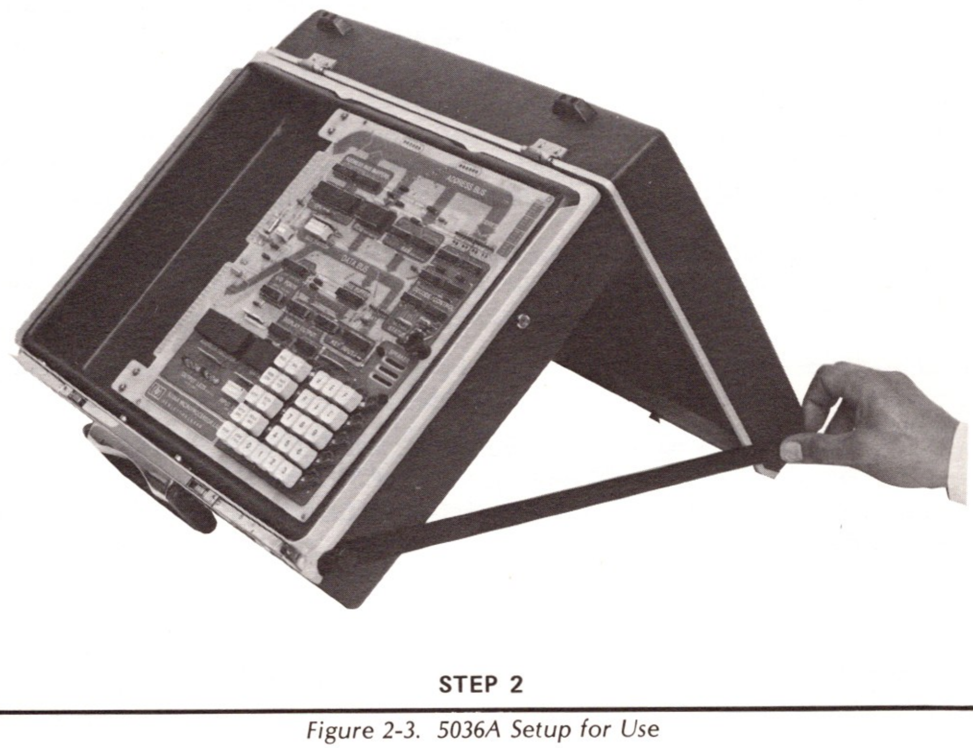
2-14. ALTITUDE. The 5036A may be operated at altitudes up to 4,600 metres (15,000 feet).

2-15. Setup

2-16. To set up the 5036A for operation, remove the top cover of the case and re-install as shown in *Figure 2-3.* Connect the strap as shown. Refer to paragraphs 2-6 through 2-10 prior to connecting the power cord. Refer to the Practical Microprocessors textbook for information on use of the 5036A.



STEP 1



STEP 2

Figure 2-3. 5036A Setup for Use

2-17. STORAGE AND SHIPMENT

2-18. Environment

2-19. The instrument may be stored or shipped in environments within the following limits:

Temperature .... −40°C to +75°C
Humidity .... Up to 95%
Altitude .... 4,600 metres (15,000 feet)

2-20. The instrument should also be protected during storage from temperature extremes which cause condensation within the instrument.

2-21. Packaging

2-22. ORIGINAL PACKAGING. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-23. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

CAUTION

THE 5036A IS NOT DESIGNED TO BE SHIPPED AS BAGGAGE ON AIRLINES OR OTHER MODES OF TRANSPORTATION. FOLLOW THE INSTRUCTIONS ON PACKAGING (ABOVE) BEFORE SHIPPING.

SECTION III
THEORY OF OPERATION

3-1. INTRODUCTION

3-2. This section contains a block diagram description of the overall operation of the 5036A, followed by a detailed circuit description in reference to the schematic diagram. A description of interrupts, the multiplexed bus, control signals, microprocessor timing, and peripheral circuits is included.

3-3. BLOCK DIAGRAM DESCRIPTION

3-4. A simplified block diagram of the microcomputer is shown in *Figure 3-1*. The three main functional blocks are the microprocessor, the memory, and the I/O ports. There are three groups of signals which interconnect the blocks: address, data, and control. Addresses are output only by the microprocessor, and specify the location in memory (or the particular I/O port) that the processor reads data from or writes data to. The bidirectional data lines carry the actual data to be read or written to or from the processor. The control lines keep the whole system operating together and specify whether the current operation is a read or a write and whether it is referring to memory or an I/O port.

3-5. Data Bus

3-6. The data bus is a bidirectional three-state bus. The bus consists of 8 lines, therefore, each talker must have eight drivers (one for each line), and each receiver must have eight inputs. (There are some exceptions to this where only part of the bus is used.) The microprocessor and the RAM are talkers and listeners. The input ports are talkers (they take inputs from outside the system and put them on the bus), and the output ports are listeners (they take data off the bus and send it outside the system). The ROM is a talker. *Figure 3-1* shows how these devices communicate with the data bus. The microprocessor, RAM, ROM, and input ports contain three-state drivers on their outputs. The select input enables the drivers and causes the data from the selected device to appear on the data bus. The microprocessor is the controller of the system; it will ensure that no more than one device is trying to use the bus at any given time. If the microprocessor wants to read data from the ROM, for example, it would three-state its own data lines and generate the control signals required to cause the ROM's select input to be true. The ROM's outputs would then appear on the data bus, and the microprocessor would read the data off the bus. Reading the RAM or the input port is done in a similar manner.

3-7. To write data to another device (the RAM or output port), the microprocessor would first place the data to be written on its data lines. It would then generate the control signals to cause a write pulse to be sent to the appropriate device, which would then input the data from the bus.

3-8. In summary, the microcomputer's data bus is a bidirectional three-state bus. In general, data always flows through the microprocessor. To transfer data from the inut port to the RAM, for example, the microprocessor would first read the data from the input port, and then write it to the RAM. The data must be temporarily stored within the microprocessor.

3-9. The data bus is used for all transfers of data within the microcomputer. All devices share the same bus. The control logic, operating from signals generated by the microprocessor, indicates to each device when it should put data on the bus or read data from the bus.

3-10. The Address Bus

3-11. The address bus is much simpler than the data bus. The microprocessor outputs addresses, and everything else listens; it is unidirectional. Before any data transfer can take place (via the

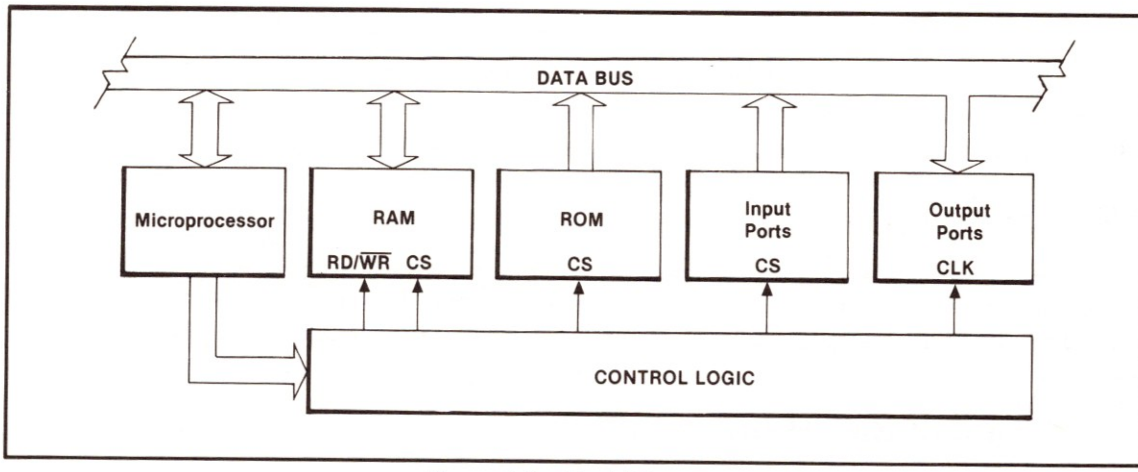


Figure 3-1. Block Diagram

data bus), the microprocessor must output an address. The address specifies the memory location (or I/O port) which the processor wishes to access. In this way the microprocessor can select any part of the system it wishes to communicate with.

3-12. The Control Bus

3-13. The address bus is used to select a particular memory location or I/O port, the data bus is then used to carry the data, and the control bus is used to control this process. The control bus consists of a number of control signals, most of which are generated by the microprocessor. The most important ones control the reading and writing of ports and memory. Other controls signals are available for accommodating interrupts, slow memories, and direct memory access.

3-14. The three main control signals generated by the microprocessor are NRD, NWR, and I0/NM. If NRD is low it indicates that a read is in progress, and the microprocessor will be expecting the device which is being addressed to put data on the data bus. If NWR is low, a write is in progress and the microprocessor will be putting data on the data bus, expecting the addressed device to be storing this data. If IO/NM is low, the operation in progress (which may be a read or write) is a memory operation. If IO/NM is high, the operation refers to an I/O port. The signal is not used in the 5036A. Refer to *Table 3-1* for a complete description of microprocessor functions, by pin number, and to the schematic diagram in *Figure 7-5.*

3-15. Addressing Structure

3-16. The 5036A does not use I/O mapping for its I/O ports. Therefore, the IO/NM line is not used for decoding. The 5036A uses memory-mapped I/O. The I/O ports are treated as addressable devices within the memory space. *Table 3-2* shows the address map. Only the first one-fourth of the address space is used, address bits 14 and 15 are always zero. This address space is then divided into eight equal sections of 2K locations each (07FF hex = 2,047 decimal). The ROM occupies the first 2K addresses (0–2047 decimal). The RAM has been assigned to the next 2K addresses.

3-17. The six-address sections following the RAM are used for I/O ports. The control port is used by the monitor to provide some special functions, which will be described later. The key data, scan, and display segment ports control the keyboard and display. The input and output ports are used for the switches and LEDs. Each of these ports carries only a single byte of data and therefore requires only one address.

3-18. This addressing scheme uses many addresses to simplify the hardware, since address space is available. The 5036A uses 16K addresses for its 2K ROM, 1K RAM, and six I/O ports. There are still 48K addresses left unused. The 5036A could have used only 2,048 + 1,024 + 6 = 3,078 addresses, which would result in more unused address space and a much more complicated address decoding circuit.

Table 3-1. Microprocessor U3 Functional Pin Definitions

Pin	
21-28	**A_8-A_{15} (Output Three-State)** Address Bus. The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes.
12-19	**AD_{0-7} (Input/Output Three-State)** Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles. Three-stated during Hold and Halt modes.
30	**ALE (Output)** Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. ALE is never three-stated.
29, 33	**S_0, S_1 (Output)** *(Not Used in 5036A)* Data Bus Status. Encoded status of the bus cycle. **S_1 S_0** 0 0 HALT 0 1 WRITE 1 0 READ 1 1 FETCH S_1 can be used as an advanced R/W status.
32	**RD (Output Three-State)** READ: Indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. Three-stated during Hold and Halt.
31	**WR (Output Three-State)** WRITE: Indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. Three-stated during Hold and Halt modes.
35	**READY (Input)** If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.
39	**HOLD (Input)** *(Not Used in 5036A)* HOLD: Indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, RD, WR, and IO/NM lines are three-stated.
38	**HLDA (Output)** *(Not Used in 5036A)* HOLD ACKNOWLEDGE: Indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low. **NOTE** HOLD and HOLD ACKNOWLEDGE are used only for fault generation (to disable the address buffers) when the 5036A is used for training in troubleshooting.

Table 3-1. Microprocessor U3 Functional Pin Definitions (Continued)

Pin

10 **INTR (Input)** *(Not Used in 5036A)*

INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

11 **INTA (Output)** *(Not Used in 5036A)*

INTERRUPT ACKNOWLEDGE: is used instead of (and has the same timing as) RD during the instruction cycle after an INTR is accepted. It can be used to activate the 8259 interrupt chip or some other interrupt port.

RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 → Highest Priority
RST 6.5
RST 5.5 → Lowest Priority *(Not Used in 5036A)*

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

6 **TRAP (Input)**

Trap interrupt is a nonmaskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or interrupt Enable. It has the highest priority of any interrupt.

36 **RESET IN (Input)**

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.

3 **RESET OUT (Output)**

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

1, 2 **X_1, X_2 (Input)**

Crystal or R/C network connections to set the internal clock generator. X_1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

37 **CLK (Output)**

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU. The period of CLK is twice the X_1, X_2 input period.

34 **IO/NM (Output)** *(Not Used in 5036A)*

IO/NM indicates whether the Read/Write is to memory or I/O. Three-stated during and Halt modes.

5 **SID (Input)** *(Not Used in 5036A)*

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

4 **SOD (Output)**

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

40 **V_{CC}**

+5 volt supply.

20 **V_{SS}**

Ground reference.

Table 3-2. System Memory Map

Bit: 15	14	13	12	11	10	9	8	Address in hex	Device	
	Upper half of address in binary									
0	0	0	0	0	0	0	0	0 0 0 0	ROM	Memory
0	0	0	0	0	1	1	1	0 7 F F		
0	0	0	0	1		0	0	0 8 0 0	RAM	
0	0	0	0	1		1	1	0 F F F		
0	0	0	1	0	0	0	0	1 0 0 0	CONTROL	I/O
0	0	0	1	0	1	1	1	1 7 F F		
0	0	0	1	1	0	0	0	1 8 0 0	KEY DATA	
0	0	0	1	1	1	1	1	1 F F F		
0	0	1	0	0	0	0	0	2 0 0 0	INPUT PORT	
0	0	1	0	0	1	1	1	2 7 F F		
0	0	1	0	1	0	0	0	2 8 0 0	SCAN (Kbd + Display)	
0	0	1	0	1	1	1	1	2 F F F		
0	0	1	1	0	0	0	0	3 0 0 0	OUTPUT PORT	
0	0	1	1	0	1	1	1	3 7 F F		
0	0	1	1	1	0	0	0	3 8 0 0	DISPLAY SEGMENTS	
0	0	1	1	1	1	1	1	3 F F F		
0	1	0	0	0	0	0	0	4 0 0 0	NOT USED	
1	1	1	1	1	1	1	1	F F F F		

3-19. DETAILED CIRCUIT THEORY

3-20. Decoding

3-21. *Figure 7-5* shows address decoder U7 and associated control circuitry. There are two things to note in this decoding: (1) some of the read/write control is mixed with the decoding, and (2) there is a special circuit for "RAM write protect".

3-22. The binary addresses listed in *Figure 7-5* show that the A11, A12, and A13 lines specify which section is being addressed. Therefore, these lines are used to provide the binary select inputs to U7 (binary to one-of-eight decoders). This provides eight separate outputs, one for each of the 2K byte blocks in use.

3-23. U7 has three enable inputs, two that are active low and one that is active high, which must all be true to allow any of the outputs to be true. The address decoding is completed by connecting the A14 and A15 lines to the two active low enables. This will prevent any of the outputs from being true, unless both A14 and A15 are low. This scheme allows for very simple address decoding circuitry. This simplicity is a direct consequence of the fact that each device was assigned a block of addresses of equal length.

3-24. Control Circuitry

3-25. The read/write control gating is distributed throughout the circuitry, using the enables on the decoder, the memory devices, and the I/O ports to reduce the number of gates required. The decoder's third enable input is connected to a gate which generates the OR of NRD and NWR. This has the effect of allowing the device select output of U7 to be true only when either a read or a write is in progress. This is necessary because the address bus will not contain meaningful information if neither NRD nor NWR are true.

3-26. In addition, the ROM and the input ports are to be selected only if a read is being performed. If they respond to either a read or a write, a "bus conflict" could occur. For example, if a write to the ROM was performed the microprocessor would put data on the data bus to be written to the ROM. It cannot, of course, write to the ROM, and if the ROM was allowed to be enabled by a write then it will also put data on the data bus, which is an unacceptable situation. To solve this problem, U11C ANDs the NRD signal with the device select. This is shown in *Figure 7-5* for the KYRD port, but not for the ROM and IN ports. The ROM and IN port chips each have two enables, so one is used for the device select and one for NRD. This effectively ANDs the NRD signal with the device select.

3-27. For the output ports, the situation is slightly different. In an attempt to read an output port (which is not a meaningful operation), a write will be performed instead, and the port will be loaded with invalid data. This is acceptable, since the software should know not to do this, and even if it does, no real damage will be caused. This is in contrast to the situation of writing to an input port, which caues a hardware conflict and must not be allowed. Therefore, it is not necessary to AND the NWR signal with the device selects for the output ports.

3-28. The RAM's device select should be true when a read or write to the RAM's address space is in progress. The gate (U11A) on the RAM's device select line is for the write protect circuit, which will be described in the following paragraphs.

3-29. RAM Write Protect Crcuitry

3-30. The write protect circuitry helps prevent the RAM's contents from being accidentally lost. A programming error may result in the microprocessor running wild (usually by interpreting data as an instruction), and often this will result in incorrect data being written into the RAM. To prevent this, the 5036A contains control latch U8. The output of this latch provides the NPROT input. When the latch is set, the RAM will be protected. The monitor will set the protect latch whenever a program is running. Otherwise, it is reset, so that data may be stored in the RAM.

3-31. Because the program may want to use the RAM to store data during program execution, only the first three-fourths of the RAM is protected. A8 and A9 indicate which fourth of the RAM is being addressed; if they are both high, then the last quarter is being addressed, and the memory will not be protected.

3-32. As shown in *Figure 7-5,* A8 and A9 are ANDed together in U9D, and the result is then ORed with NRD and NPROT in U11B. This produces the RAM enable signal, which will be true if A8 and A9 are high, if a read is in progress, or if the protect latch is not set. If the protect latch is set, then the RAM will be disabled unless a read is in progress, or if A8 and A9 are high.

3-33. RAMs

3-34. The 5036A uses 4K-bit static RAMs (U5 and U6). Each contains 1K 4-bit words, so two must be used to get an 8-bit word. Two RAMs therefore provide 1K bytes.

3-35. *Figure 7-5* shows the RAM circuitry. The address and control pins of both chips are connected together. U5 connects to data lines 0-3, and U6 connects to lines 4-7. The two RAMs thus act as one 1K × 8-bit memory.

3-36. ROM

3-37. ROM U4 contains 2K bytes, and is mask-programmed. The low-order 11 address lines (A0-A10) supply an address to the ROM which drives the data bus. The two selects must both be true for the output three-state drivers to be enabled. The ROM will therefore only drive the data bus if the ROM select is true and the operation is a read.

3-38. Speaker

3-39. The speaker is driven by the microprocessor's serial output. This is, in effect, a one-bit output port. *Figure 7-5* shows how the speaker is connected. The U3 SOD output is buffered by U18A and sent to the edge connector for use by external hardware. It is then buffered again to drive the speaker. The speaker draws so much current that the signal at the edge connector would not have valid logic levels if the speaker buffer were not used. A 100-ohm resistor in series with the speaker limits the current to levels which will not damage the buffer. Note that the other end of the speaker is connected to +5V, not to ground. This is because the TTL buffer can sink more current than it can source, i.e., it can pull more current through the speaker than it could push. All of the actual tone generation is performed by the software. The "beep" program turns the serial output on and off several hundred times a second, which feeds a several-hundred-hertz squarewave to the speaker.

3-40. The Control Port

3-41. The control port is used by the microprocessor for sending signals to special circuits as described in the following paragraphs.

3-42. Control Port U8 is a 4-bit register clocked by the control port select signal, which is generated by address decoder U7. This is similar to the other output ports. The unusual thing about this port is that the data inputs are connected to the address bus, instead of the data bus. Therefore, the data written to the port is independent of the state of the data bus. The control port will be selected by any address from 1000 to 17FF. This allows the 11 low-order address lines to contain any value, and still select this port. Note that AØ, A1, and A2 provide the data inputs. The data sent to the port is therefore determined by the address used to write to the port. For example, a write to address 1000 would clear all the bits. A write to address 1001 would set the PROT bit, and a write to 1004 would be the INSS bit

3-43. The reason for this "trick" technique is that it simplifies the software. Since it doesn't matter what data is sent to the port (only the address matters), the software does not need to set up a value before it writes to the port. The hardware is no more complicated than if the traditional arrangement were used.

3-44. The PROT bit of this port is used to control the memory protect circuit. If this bit is set, the first three-fourths of the RAM will be "write protected" as described in paragraph 3-29. The other two bits are used to control the single-step circuitry.

3-45. Interrupts

3-46. Interrupts provide a means for hardware external to the microprocessor to request immediate action by the processor. They allow the usual program flow to be interrupted, and cause control to be transferred to a special routine. The following paragraphs describe the hardware required to initiate an interrupt, assuming that the interrupt in question has been enabled by the software.

3-47. There are two groups of interrupts available on the microprocessor: TRAP, RST 5.5, 6.5, and 7.5, which are controlled by the individual pins on the microprocessor, and RST 1, 2, 3, 4, 5, 6, and 7, which are controlled via INTR (Interrupt Request) and INTA (Interrupt Acknowledge). The first group, which is used in the 5036A, is described in the next paragraph. The second group of interrupts is not used in the 5036A.

3-48. All that is required to initiate one of the interrupts in the first group is to apply a signal to the corresponding pin on the microprocessor. The RST 5.5 and 6.5 inputs will respond to a high level (logic 1). The RST 7.5 input will respond only to a positive edge, i.e., a transition from low to high. The TRAP input will respond to a high level, but will not be acknowledged a second time until it has gone low and then high again. The RST 5.5 input is not used in the 5036A.

3-49. The 5036A uses the TRAP input for the RESET key, the RST 6.5 input for the INTRPT key, and the RST 7.5 input for the SA (Signature Analysis) switch. Signature analysis is described in paragraph 7-36.

3-50. An OR gate (with active low inputs actually NAND gate U9A) is used to allow the single-step circuitry to access the TRAP input. The 100-ohm resistor and the capacitor are used to debounce the RESET switch, which is necessary so that it will cause only one interrupt. With the other interrupts this is not necessary, because the software can disable the interrupt as soon as it is acknowledged, thus preventing a second interrupt. The TRAP input cannot be disabled, so it must be debounced by the hardware.

3-51. Priorities

3-52. Some allowances must be made for the fact that more than one interrupt may be requested simultaneously. Each interrupt is assigned a priority, and the interrupt with the highest priority will be acknowledged first. TRAP has the highest priority, followed by RST 7.5, 6.5, and 5.5 (in that order). INTR has the lowest priority. RST 5.5 is not used in the 5036A.

3-53. The Multiplexed Bus

3-54. As shown in *Figure 7-5,*U3 microprocessor multiplexes the data bus with the lower half of the address bus. An 8-bit address bus carries the upper half of the address, and an 8-bit address/data bus carries the data and the lower half of the address.

3-55. The Address Latch Enable (ALE) signal is generated by the microprocessor to indicate when the address/data bus contains an address. This signal is used to latch the bus contents and generate the lower half of the address bus.

3-56. U2 is an 8-bit latch with three-state outputs. It latches the address information off the address/data bus at the negative edge of ALE (the inverter U2 is necessary to select this edge). U1 is a simple three-state buffer, and is not really part of the demultiplexing.

3-57. *Figure 3-2* shows a generalized picture of the bus timing. The A8-A15 lines always contain the high-order address byte. At the beginning of each memory cycle, the low-order address byte is placed on the address/data bus. The trailing edge (high-to-low transition) of ALE indicates that this is present, and causes the demultiplexing latch to store the low-order byte of address.

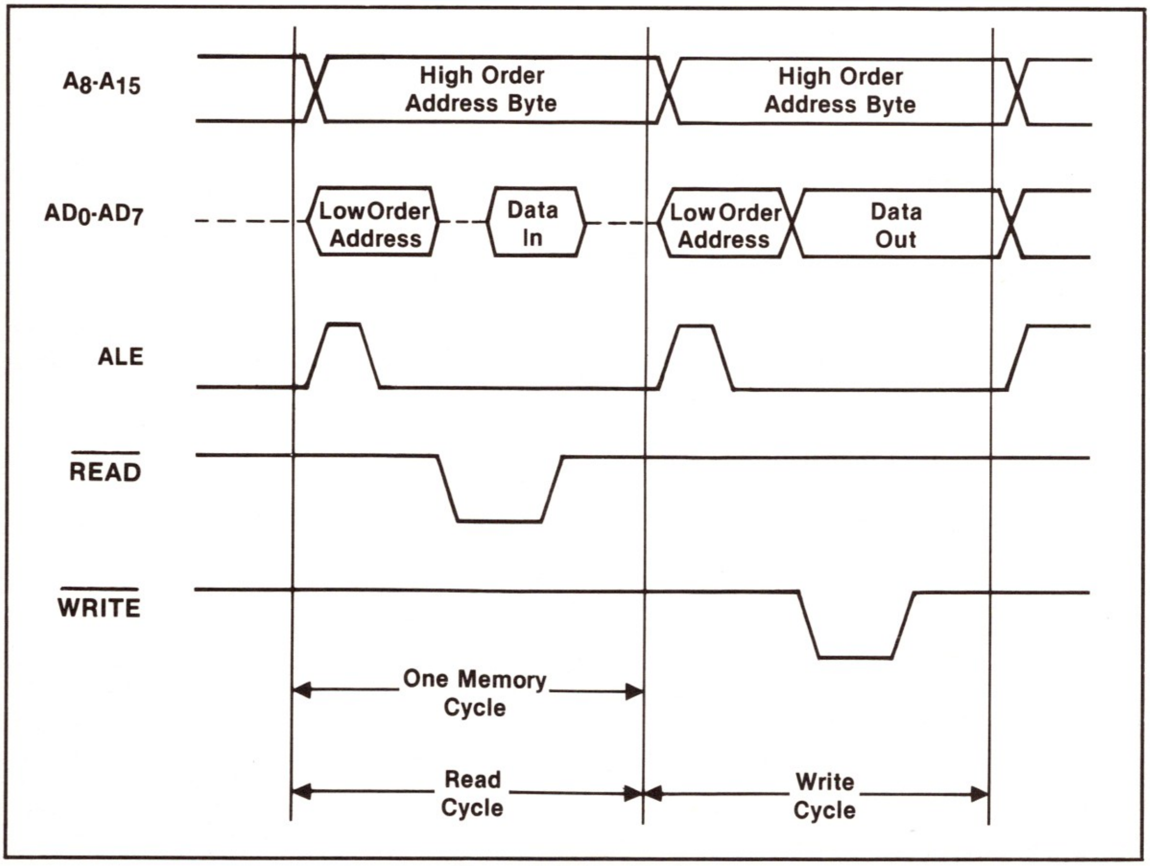


Figure 3-2. Bus Timing

3-58. The address is then removed from the address/data bus to allow the data transfer to take place. If a read operation is in progress, the microprocessor will issue a read signal, and the addressed memory of I/O device will place the data on the address/data bus. At the trailing edge of NRD, the microprocessor will read the data off the bus.

3-59. The write cycle is similar, except that the direction of the data transfer is reversed. At the beginning of the cycle, the low-order address byte is placed on the address/data bus, and ALE is pulsed. Then the microprocessor issues a write pulse, and places the data on the address/data bus. At the trailing edge of NWR, the addressed memory device will store the data from the bus.

3-60. With the addition of demultiplexing latch U2, the buses become identical to nonmultiplexed buses. The address/data bus simply becomes the data bus. Note that it will contain address information early in each memory cycle. This is significant, however, since the data bus is not in use at this time (neither NRD nor NWR is true).

3-61. Reset

3-62. The RESET pin (36) on the U3 microprocessor is used for power-up initialization. When a low level is applied to this pin, the microprocessor's internal circuitry is cleared. The program counter is set to 0000, so program execution beings from that address. The power-up initialization routine begins there.

3-63. A resistor is used to pull the RESET line high, and a capacitor provides an automatic power-on pulse. When power is first applied, the capacitor is discharged and a low level is applied to the RESET input. As long as this remains low, the processor will remain reset. When the capacitor charges up to the threshold of the input (which has a Schmitt trigger to eliminate noise), the processor will begin executing the program at 0000. Note that the 5036A's RESET key goes to TRAP.

3-64. Status

3-65. The Status output, pins 29 and 33 of Microprocessor U3 are not used in the 5036A.

3-66. Ready

3-67. The Ready input, U3(35), when brought low, will cause the microprocessor to enter a "wait" state. The buses will not be three-stated, but will remain at their current status until Ready is brought high again. The Ready input is used for the hardware (single) step mode. This mode allows observation of the address, data and status LEDs for each step of a program.

3-68. Hold

3-69. The Hold (input) U3(39) and Hold Acknowledge (output) U3(38) are not used in the 5036A.

3-70. Timing

3-71. There are many complicated timing relationships which must be satisfied for the microprocessor to operate correctly. *Figure 3-3* shows the timing for a write operation. The address must be stable for some period of time, called the access time, before any operation may be performed. This allows the memory's internal address decoders to select the specified memory cell. The data must then be stable for some time before the write occurs, and this is called set-up time. The data must also be stable for some time after the write, which is called hold time. Finally, the write pulse must have some minimum duration.

3-72. *Figure 3-4* shows the timing for a read operation. As with the write operation, the address must be stable for some time to allow the memory's internal decoders to settle. A read pulse is then generated, and after some amount of time (the data access time) the memory will place the indicated data on the data bus. This data must be stable for the set-up time before the rising edge of NRD, when the data is read into the microprocessor. The data must remain stable for the data hold time.

3-73. *Figure 3-5* shows the CPU timing for a typical instruction. The basic unit of time is the state, which is one clock period. A machine cycle consists of from three to six states. Most simple operations (such as moving one register to another or reading a memory location) requires one machine cycle. The instruction cycle is the time to execute an entire instruction, and consists of one to five machine cycles.

3-74. *Figure 3-6* gives the complete system timing for an OUT instruction. States are denoted by T1, T2, etc., and machine cycles by M1, M2, etc. This diagram combines all the timing discussed earlier; the multiplexed bus, reads, and writes. In addition, the status (S0 and S1) lines are shown (these lines are not used in the 5036A).

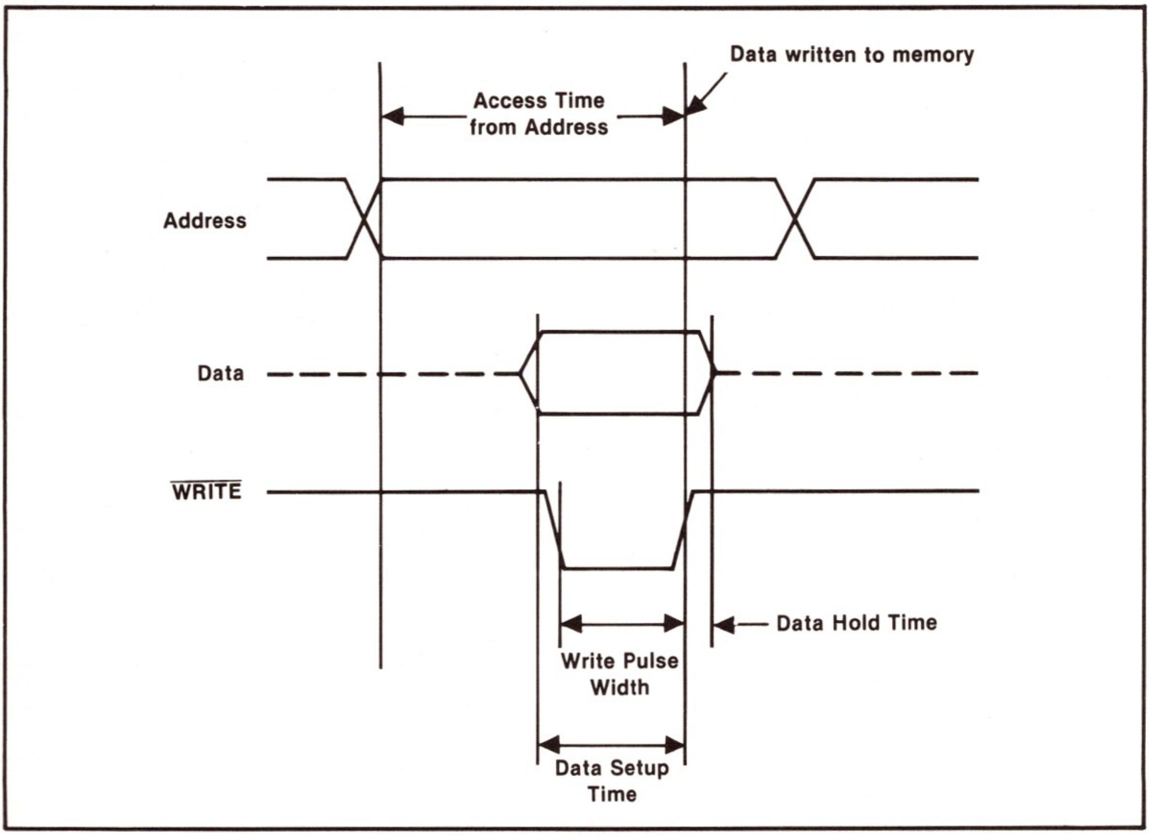


Figure 3-3. Write Timing

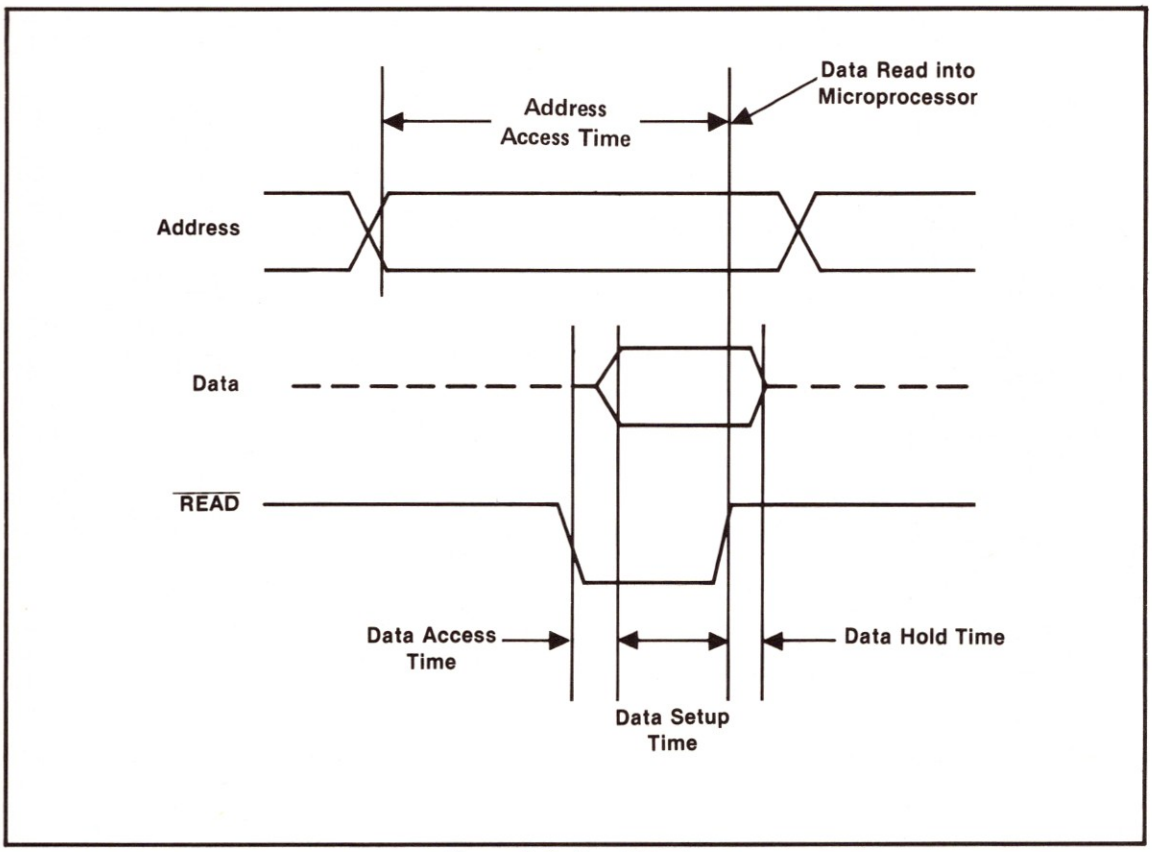


Figure 3-4. Read Timing

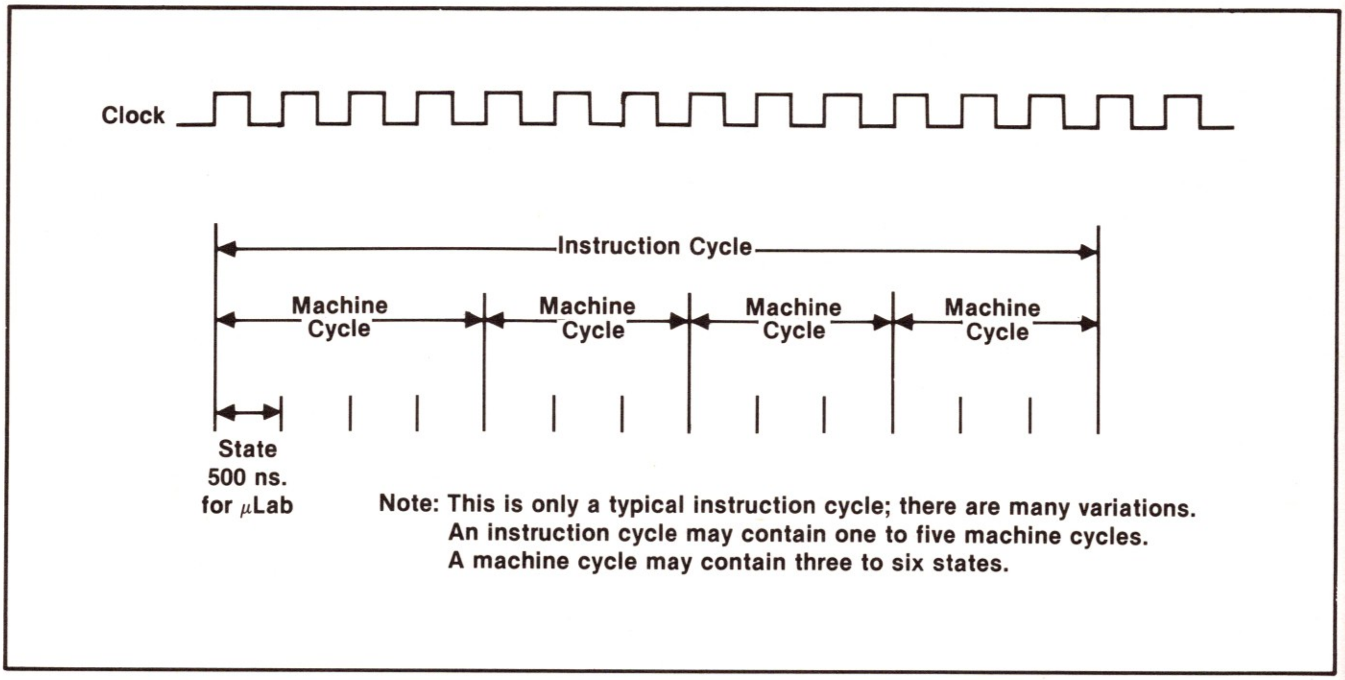


Figure 3-5. Summary of Microprocessor Timing

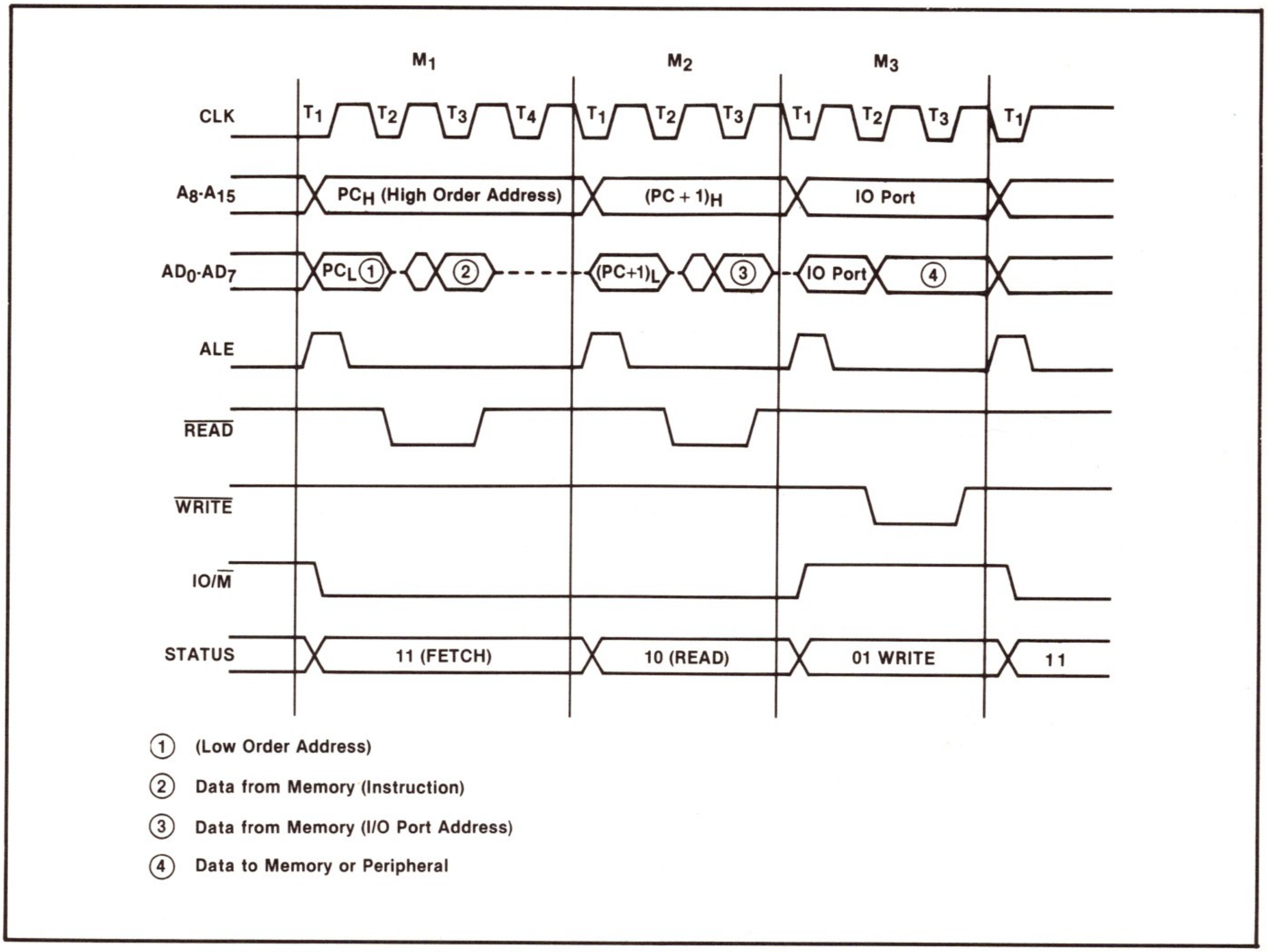


Figure 3-6. Timing for the Fetch and Execution of an OUT Instruction

3-75. In the first machine cycle (M1), the opcode is fetched from the memory. In M2, the second byte of the instruction (the port address) is read from the memory. In M3, the instruction is executed, data is written to the I/O port.

3-76. All instructions require one machine cycle to fetch the opcode. For simple instructions which do not use the memory or I/O (such as MOV A, B), the execution can be performed during the first (and only) machine cycle. For multiple-byte instructions (such as MVI A,7 or STA 0837), one machine cycle will be required to read each byte of the instruction. If the instruction execution requires a reference to memory or I/O, the execution will require an additional cycle. Some complex operations (such as DAD) use an extra machine cycle for executing the instruction, even though all the operation is internal to the microprocessor.

3-77. The 5036A provides a demonstration of these cycles via the step mode. HDWR STEP steps one machine cycle at a time, and INSTR STEP steps one instruction cycle.

3-78. For additional information on operation and programming, refer to the Practical Microprocessors manual supplied with the 5036A.

3-79. Peripherals

3-80. For the microcomputer to be of any use, there must be some operator interface. Usually an input and an output device are required. These connect to the microcomputer through I/O ports, and since they are not directly involved in the operation of the microprocessor, they are called peripherals.

3-81. The 5036A has two simple peripherals: the input port slide switches and the output port LEDs. *Figure 7-5* shows how these are connected. The ports and control circuitry were described previously. The switches at the inputs of the input port will cause the input to be low if the switch is closed. If the switch is open, the resistor will pull the input high. The output port simply has each output driving an LED. Resistors limit the current. When the output is low, current will be drawn through the LED and it will be illuminated.

3-82. Keyboard and Display

3-83. While the switches and LEDs are simple and functional, many applications require something easier for the operator to use. Two very common microcomputer peripherals are keyboards and displays, both of which are used in the 5036A. The basic operation of these peripherals is described in the following paragraphs.

3-84. An important technique, which is used in both of these peripherals, is scanning. The key board has 26 keys as listed in paragraph 3-90. To connect each key to an input port bit would require four 8-bit input ports. By a multiplexing arrangement, we can interface up to 256 keys using only two ports. *Figure 7-5* shows the keyboard interface. The keys are arranged in a matrix, interconnecting column lines and row lines. An output port (U17) drives the columns, and an input port (U18B) reads the rows. The monitor program scans the keyboard. The output port is set so that one line is low and all others are high, and then the input port is read. If any of the keys in the column whose line is low are pressed, then the row line which that key is on will be forced low. Therefore, that input port bit will be low. If no keys are pressed, the input port lines are all pulled up to a high level. The program then knows which column the key is in (from which output port bit it set low) and which row it is in (from which input port bit is low). This uniquely identifies the key.

3-85. To check all the keys, each output port bit must be set low in turn. Thus the keys are scanned. At each step only four keys are checked. The process is so fast, however, that the entire keyboard can be checked, four keys at a time, in much less time than the fastest possible manual key pressing.

3-86. The display also uses a scanning technique. Although the 5036A display has six digits, only one is actually on at any instant. They are each turned on in sequence, but this happens so fast that they appear to all be on at the same time. Each display digit consists of a seven-segment LED and has seven segment connections and a common. There is also a connection for the decimal point, which is treated as an eighth segment. A character is displayed by putting a low level on the common, and a high level on the segment inputs corresponding to the segments we wish to illuminate.

3-87. To interface the displays without using an inordinate number of output port lines, the segment inputs to each display are bused together, as shown in *Figure 7-5*. One 8-bit output port (U19) then supplies segment information to all of the displays. Another output port (U20) is used to drive the commons of each display, so the microprocessor may select which digit should be on.

3-88. Software is required to run the display, as follows. First, the segment information for digit 1 is sent to the segment port. Then the digit port is set to activate only digit 1. After allowing digit 1 to be on for some amount of time, it is turned off (via the digit port). Then the segment information for digit 1 is sent to the segment port, and digit 2 is enabled by the digit port. This process repeats indefinitely, with each digit being illuminated in turn.

3-89. 5036A KEYBOARD

3-90. The 5036A keyboard keys and functions are as follows:

EXECUTION CONTROL GROUP		MEMORY CONTROL GROUP	
RUN	RUN: Initiates a program	STORE /INCR	STORE/INCREMENT: Stores data in a user memory location or register and advances address by one.
HDWR STEP	HARDWARE STEP: Single steps a program one machine cycle at a time.	DECR	DECREMENT: Decrements address by one.
INSTR STEP	INSTRUCTION STEP: Steps a program through one complete instruction at a time.	FETCH ADRS	FETCH ADDRESS: Allows an address and its contents to be called and displayed.
RESET	RESET: Resets the Lab or stops a program.	FETCH REG	FETCH REGISTER: Allows A register to be displayed with its contents. Pressing Store/Increment allows each of the 8085's other registers to be viewed in turn or modified.
INTRPT	INTERRUPT: Provides a user-defined hardware interrupt to the system.	FETCH P C	FETCH PROGRAM COUNTER: Displays contents of the program counter.

HEXADECIMAL NUMERALS															
0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F

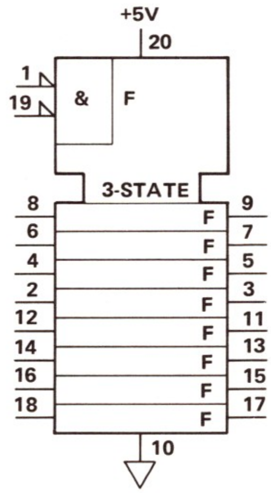
3-91. LOGIC SYMBOLS

3-92. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std. 91-1973). This standard supersedes MIL-STD-806B. The specific symbols used in this manual are described in detail in the following paragraphs. For additional information on general symbols refer to training manual, Logic Symbology, HP Part Number 5951-6116. The training manual may be ordered from the HP Parts Center, Mountain View, California.

Reference Designator
U1, U13, U14
Part Number
1820-1794

Description
OCTAL BUFFER

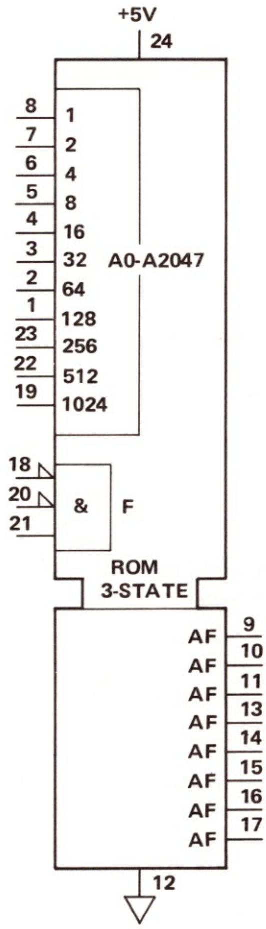
Eight buffers are enabled by pins 1 AND 19 active low. The outputs are placed in the three-state (high impedance) condition (F) by applying a high logic level to the enable pins.



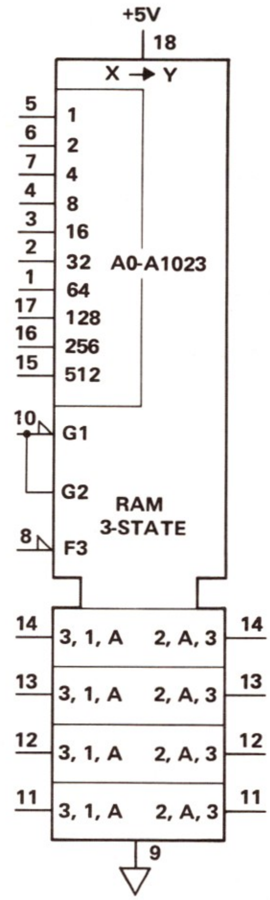
Reference Designator
U4
Part Number
1818-0498

Description
2K X8 ROM

Read-only memory with 2048 addresses containing the software that controls the microprocessor operation. Address selection is determined by the 11-bit address input in the upper left corner of the control block. The "F AND" function (pins 18 and 20 low and 21 high) enables the output. The AF output label indicates dependency on the three-state enable (F) and the memory location addressed.



Reference Designator
U5, U6
Part Number
1818-0438



Description
RAM (with identical input/output pins)

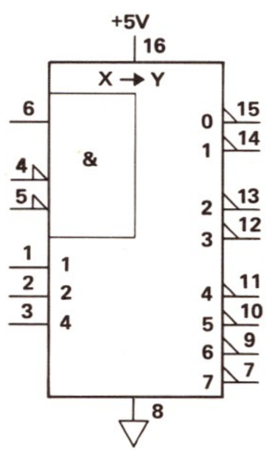
Random-Access memory with possible access to 1024 locations. Address selection is determined by the 10 address input codes in the upper left corner of the control block. These address codes are weighted to correspond to the possible addresses (A0-1023).

G1 and G2 are the read and write enables. A low on Pin 10 will enable G1 or the Read function. A high on Pin 10 will enable G2 or the Write function. F3 is the three-state enable line. A low on pin 8 will enable data to be read and written.

The input lines are noted in the lower left portion of the symbol. "3" indicates that these inputs are enabled when there is a low on F3. 1A indicates that information will be read into the chip when G1 is enabled at the memory location addressed.

The output lines are noted in the lower right portion of the symbol. "3" indicates that these outputs are enabled by a low on F3. "2" indicates that information will be written out of the chip when G2 is enabled at the memory location addressed.

Reference Designator
U7
Part Number
1820-1216



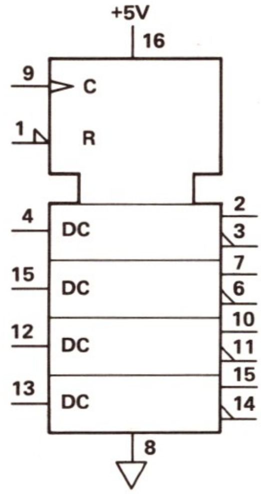
Description
DECODER

The binary-weighted inputs are decoded to provide the output when enable input pins 4 and 5 are low and 6 is high.

Reference Designator
U8
Part Number
1820-1195

Description
QUAD D-TYPE FLIP-FLOPS

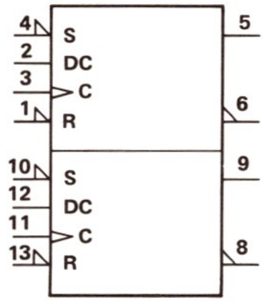
Data at the DC inputs is transferred to the outputs on the positive-going edge of the clock pulse (pin 9). A low signal at the reset (pin 1) will clear all FFs.



Reference Designator
U10
Part Number
1820-1112
SN74LS74

Description
DUAL D-TYPE FLIP-FLOP

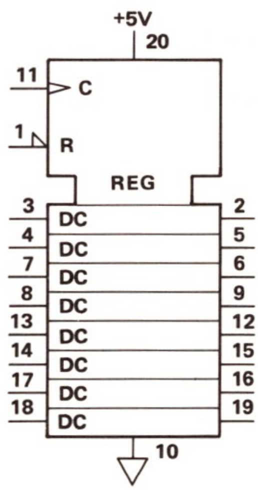
The dual D-type Flip-Flop consists of two independent D-type flip-flops. The information present at the data (D_C) input is transferred to the active-high and active-low outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next low-to-high transition of the clock input. The set (S) and reset (R) inputs override all other input conditions when (S) is low, the active-high output is forced high; when reset (R) is low, the active-high output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs at the set and reset will force both the active-low and active-high outputs to go high at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held low. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the high state.



Reference Designator
U15, U16, U17
Part Number
1820-1730
74LS273

Description
OCTAL D-TYPE FLIP-FLOP

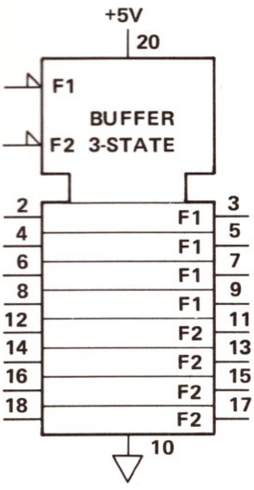
Data at the D_C input of each flip-flop is transferred to the output on the positive-going edge of the clock pulse. A low signal at the reset (pin 1) will clear all flip-flops.



Reference Designator
U18
Part Number
1820-1759
81LS97

Description
THREE-STATE BUFFERS

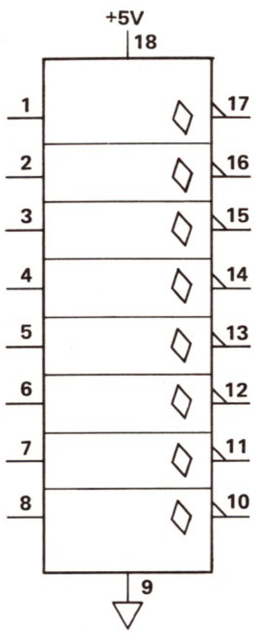
Four buffers are enabled by each common control input, F1 and F2, when low. The outputs are placed in the three-state (high-impedance) condition by a high logic level on the control pin.



Reference Designator
U19
Part Number
1820-2138
DS8871

Description
LED CATHODE DRIVER

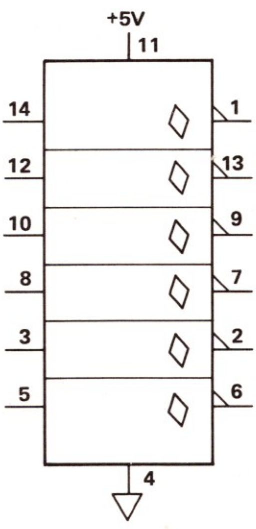
Eight-digit driver interfaces the buffered data bus and the display to supply segment information to all digits. The open collector output (◊) sinks current.



Reference Designator
U20
Part Number
1820-1231
SN75492N

Description
U20 DIGIT DRIVER

Six-digit driver interfaces the buffered data bus and display to supply digit scan information. The open collector output (◊) sinks current.



SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the electrical performance of the 5036A. All tests can be performed using the controls and indicators on the 5036A with the exception of the +5 volt check and the clock frequency check which require use of a voltmeter and a frequency counter.

4-3. PERFORMANCE TEST PROCEDURES

4-4. Test the performance of the 5036A by performing the step-by-step procedures listed in *Table 4-1*. If normal indications are not received, refer to the troubleshooting procedures, paragraph 7-31.

Table 4-1. Performance Test

NOTE

Apply power and using 3476A Digital Voltmeter, check +5V terminals for +5 (=0.25) volts. Using 5381 Frequency Counter, check U3, pin 37 for 2 MHz (±0.05%) clock signal. Proceed as follows:

Action	Indication
With BUS, INPUT, S.A. and FR switches in down position, place LINE switch to OFF, then ON.	ADDRESS/REGISTER and DATA display shows all 8's and decimal points and all OUTPUT LED's light momentarily. Speaker beeps once. Display changes to uLAb UP and OUTPUT LEDs go off.
Place all BUS SWITCH sections to up position. Place adjacent test switch to FREERUN (FR).	All ADDRESS LEDs on or flickering. DATA LEDs all flickering. READ LED on. WRITE LED off. ROM, RAM, INPUT, and OUTPUT STATUS LEDs flickering. Display off. OUTPUT LEDs off.
Place test switch to NORM and all sections of BUS SWITCH down. Press the RESET key twice.	Display: uLAb UP
Press FETCH ADRS key	Display: _ _ _ _ ▮▮
Press 0, 4, d, 7 keys	Display: 04d7 3A
Press each key 0 through F	Rightmost Display Digit: Key pressed shown.
Press DECR key	Display: 04d6 04
Press STORE/INCR key	Display: 04d7 3A
Press INSTR STEP key	Display: 04dA 32
Press HDWR STEP key	Display:Blank
Press RESET key	Display: 04dd C3

Note: ▮ indicates blank digit

Table 4-1. Performance Test (Continued)

Action	Indication
Press FETCH REG key	Display: ███A 00
Press FETCH PC key	Display: 04dd C3
Press RUN key. Slide each INPUT switch section up and down and observe OUTPUT LEDs.	OUTPUT LED "off" when corresponding switch up and "on" when switch down.

Note: █ indicates blank digit

SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION

5-2. This section contains information for ordering replacement parts. *Table 5-1* lists parts in alphanumerical order of their reference designators and indicates the description and HP Part Number of each part, together with any applicable notes. The tables includes the following information.

a. Hewlett-Packard part number.
b. Part number check digit (CD).
c. Total quantity used in the instrument (Qty column).
d. Description of part (see abbreviations below).
e. Typical manufacturer of the part in a five-digit code; see list of manufacturers in *Table 5-2*.
f. Manufacturer's part number.

REFERENCE DESIGNATIONS

A	= assembly
AT	= attenuator; isolator; termination
B	= fan; motor
BT	= battery
C	= capacitor
CP	= coupler
CR	= diode; diode thyristor; varactor
DC	= directional coupler
DL	= delay line
DS	= annunciator; signaling device (audible or visual); lamp; LED
E	= micellaneous electrical part
F	= fuse
FL	= filter
H	= hardware
HY	= circulator
J	= electrical connector (stationary portion); jack
K	= relay
L	= coil; inductor
M	= meter
MP	= miscellaneous mechanical part
P	= electrical connector (movable portion); plug
Q	= transistor; SCR; triode thyristor
R	= resistor
RT	= thermistor
S	= switch
T	= transformer
TB	= terminal board
TC	= thermocouple
TP	= test point
U	= integrated circuit; microcircuit
V	= electron tube
VR	= voltage regulator; breakdown diode
W	= cable; transmission path; wire
X	= socket
Y	= crystal unit-piezo-electric
Z	= tuned cavity; tuned circuit

ABBREVIATIONS

A	= ampere
ac	= alternating current
ACCESS	= accessory
ADJ	= adjustment
A/D	= analog-to-digital
AF	= audio frequency
AFC	= automatic frequency control
AGC	= automatic gain control
AL	= aluminum
ALC	= automatic level control
AM	= amplitude modulation
AMPL	= amplifier
APC	= automatic phase control
ASSY	= assembly
AUX	= auxiliary
avg	= average
AWG	= american wire gauge
BAL	= balance
BCD	= binary coded decimal
BD	= board
BE CU	= beryllium copper
BFO	= beat frequency oscillator
BH	= binder head
BKDN	= breakdown
BP	= bandpass
BPF	= bandpass filter
BRS	= brass
BWO	= backward-wave oscillator
CAL	= calibrate
ccw	= counterclockwise
CER	= ceramic
CHAN	= channel
cm	= centimeter
CMO	= coaxial
COEF	= coefficient
COM	= common
COMP	= composition
COMPL	= complete
CONN	= connector
CP	= cadmium plate
CRT	= cathode-ray tube
CTL	= complementary transistor logic
CW	= continuous wave
cw	= clockwise
D/A	= digital-to-analog
dB	= decibel
dBm	= decibel referred to 1 mW
dc	= direct current
deg	= degree (temperature interval or difference)
...°	= degree (plane angle)
°C	= degree Celsius (centrigrade)
°F	= degree Fahrenheit
°K	= degree Kelvin
DEPC	= deposited carbon
DET	= detector
diam	= diameter
DIA	= diameter (used in parts list)
DIFF AMPL	= differential amplifier
div	= division
DPDT	= double-pole, double-throw
DR	= drive
DSB	= double sideband
DTL	= diode transistor logic
DVM	= digital voltmeter
ECL	= emitter coupled logic

ABBREVIATIONS (CONTINUED)

EMF	= electromotive force
EDP	= electronic data processing
ELECT	= electrolytic
ENCAP	= encapsulated
EXT	= external
F	= farad
FET	= field-effect transistor
F/F	= flip-flop
FH	= flat head
FOL H	= fillister head
FM	= frequency modulation
FP	= front panel
FREQ	= frequency
FXD	= fixed
g	= gram
GE	= germanium
GHz	= gigahertz
GL	= glass
GND	= ground(ed)
H	= henry
h	= hour
HET	= heterodyne
HEX	= hexagonal
HD	= head
HDW	= hardware
HF	= high frequency
HG	= mercury
HI	= high
HP	= Hewlett-Packard
HPF	= high pass filter
HR	= hour (used in parts list)
HV	= high voltage
Hz	= Hertz
IC	= integrated circuit
ID	= inside diameter
IF	= intermediate frequency
IMPG	= impregnated
in	= inch
INCD	= incandescent
INCL	= include(s)
INP	= input
INS	= insulation
INT	= internal
kg	= kilogram
kHz	= kilohertz
kΩ	= kilohm
kV	= kilovolt
lb	= pound
LC	= inductance-capacitance
LED	= light-emitting diode
LF	= low frequency
LG	= long
LH	= left hand
LIM	= limit
LIN	= linear taper (used in parts list)
lin	= linear
LK WASH	= lockwasher
LO	= low; local oscillator
LOG	= logarithmic taper (used in parts list)
log	= logarithm(ic)
LPF	= low pass filter
LV	= low voltage
m	= meter (distance)
mA	= milliampere
MAX	= maximum
MΩ	= megohm
MEG	= meg (10^6) (used in parts list)
MET FLM	= metal film
MET OX	= metal oxide
MF	= medium frequency; microfared (used in parts list)
MFR	= manufacturer
mg	= milligram
MHz	= megahertz
mH	= millihenry
mho	= mho
MIN	= minimum
min	= minute (time)
...′	= minute (plane angle)
MINAT	= miniature
mm	= millimeter
MOD	= modulator
MOM	= momentary
MOS	= metal-oxide semi-conductor
ms	= millisecond
MTG	= mounting
MTR	= meter (indicating device)
mV	= millivolt
mVac	= millivolt, ac
mVdc	= millivolt, dc
mVpk	= millivolt, peak
mVp-p	= millivolt, peak-to-peak
mVrms	= millivolt, rms
mW	= milliwatt
MUX	= multiplex
MY	= mylar
μA	= microampere
μF	= microfarad
μH	= microhenry
μmho	= micromho
μs	= microsecond
μV	= microvolt
μVac	= microvolt, ac
μVdc	= microvolt, dc
μVpk	= microvolt, peak
μVp-p	= microvolt, peak-to-peak
μVrms	= microvolt, rms
μW	= microwatt
nA	= nanoampere
NC	= no connection
N/C	= normally closed
NE	= neon
NEG	= negative
nF	= nanofarad
NI PL	= nickel plate
N/O	= normally open
NOM	= nominal
NORM	= normal
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NRFR	= not recommended for field replacement
NSR	= not separately replaceable
ns	= nanosecond
nW	= nanowatt
OBD	= order by description
OD	= outside diameter
OH	= oval head
OP AMPL	= operational amplifier
OPT	= option
OSC	= oscillator
OX	= oxide
oz	= ounce
Ω	= ohm
P	= peak (used in parts list)
PAM	= pulse-amplitude modulation
PC	= printed circuit
PCM	= pulse-code moudulation; pulse-count modulation
PDM	= pulse-duration modulation
pF	= picofarad
PH BRZ	= phosphor bronze
PHL	= Phillips
PIN	= positive-intrinsic-negative
PIV	= peak inverse voltage
pk	= peak
PL	= phase lock
PLO	= phase lock oscillator
PM	= phase modulation
PNP	= positive-negative-positive
P/O	= part of
POLY	= polystyrene
PORC	= porcelain
POS	= positive; position(s) (used in parts list)
POSN	= position
POT	= potentiometer
p-p	= peak-to-peak
PP	= peak-to-peak (used in parts list)
PPM	= pulse-position modulation
PREAMPL	= preamplifier
PRF	= pulse-repetition frequency
PRR	= pulse repetition rate
ps	= picosecond
PT	= point
PTM	= pulse-time modulation
PWM	= pulse-width modulation
PWV	= peak working voltage
RC	= resistance capacitance
RECT	= rectifier
REF	= reference
REG	= regulated
REPL	= replaceable
RF	= radio frequency
RFI	= radio frequency interference
RH	= round head; right hand
RLC	= resistance-inductance-capacitance
RMO	= rack mount only
rms	= root-mean-square
RND	= round
ROM	= read-only memory
R&P	= rack and panel
RWV	= reverse working voltage
S	= scattering parameter
s	= second (time)
...″	= second (plane angle)
S-B	= slow-blow (fuse (used in parts list)
SCR	= silicon controlled rectifier; screw
SE	= selenium
SECT	= sections
SEMICON	= semiconductor
SHF	= superhigh frequency
SI	= silicon
SIL	= silver
SL	= slide
SNR	= signal-to-noise ratio
SPDT	= single-pole, double-throw
SPG	= spring
SR	= split ring
SPST	= single-pole, single-throw
SSB	= single sideband
SST	= stainless steel
STL	= steel
SQ	= square
SWR	= standing-wave ratio
SYNC	= synchronize
T	= timed (slow-blow fuse)
TA	= tantalum
TC	= temperature compensating
TD	= time delay
TERM	= terminal
TFT	= thin-film transistor
TGL	= toggle
THD	= thread
THRU	= through
TI	= titanium
TOL	= tolerance
TRIM	= trimmer
TSTR	= transistor
TTL	= transistor-transistor logic
TV	= television
TVI	= television interference
TWT	= traveling wave tube
U	= micro (10^{-6}) (used in parts list)
UF	= microfarad (used in parts list)
UHF	= ultrahigh frequency
UNREG	= unregulated
V	= volt
VA	= voltampere
Vac	= volts ac
VAR	= variable
VCO	= voltage-controlled oscillator
Vdc	= volts dc
VDCW	= volts dc, working (used in parts list)
V(F)	= volts, filtered
VFO	= variable-frequency oscillator
VHF	= very-high frequency
Vpk	= volts peak
Vp-p	= Volts peak-to-peak
Vrms	= volts rms
VSWR	= voltage standing wave ratio
VTO	= voltage-tuned oscillator
VTVM	= vacuum-tube voltmeter
V(X)	= volts, switched
W	= watt
W/	= with
WIV	= working inverse voltage
WW	= wirewound
W/O	= without
YIG	= yttrium-iron-garnet
Zo	= characteristic impedance

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

5-3. ORDERING INFORMATION

5-4. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

5-5. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

5-6. HP PART NUMBER ORGANIZATION

5-7. Following is a general description of the HP part number system.

5-8. Component Parts and Materials

5-9. Generally, the prefix of HP part numbers identifies the type of device. Eight-digit part numbers are used, where the four-digit prefix identifies the type of component, part, or material and the four-digit suffix indicates the specific type. Following is a list of some of the more commonly used prefixes for component parts. The list includes HP manufactured parts and purchased parts.

Prefix	Component/Part/Material	
0121–	Capacitors, Variable (mechanical)	
0122–	Capacitors, Voltage Variable (semiconductor)	
0140–	Capacitors, Fixed	Non-Electrolytic
0150–	Capacitors, Fixed	Non-Electrolytic
0160–	Capacitors, Fixed	Non-Electrolytic
0180–	Capacitors, Fixed Electrolytic	
0330–	Insulating Materials	
0340–	Insulators, Formed	
0370–	Knobs, Control	
0380–	Spacers and Standoffs	
0410–	Crystals	
0470–	Adhesives	
0490–	Relays	
0510–	Fasteners	
0674– thru 0778–	Resistors, Fixed (non wire wound)	
0811– thru 0831–	Resistors (wire wound)	
1200–	Sockets for components	
1205–	Heat Sinks	
1250–	Connectors (RF and related parts)	
1251–	Connectors (non RF and related parts)	
1410–	Bearings and Bushings	
1420–	Batteries	
1820–	Monolithic Digital Integrated Circuits	
1826–	Monolithic Linear Integrated Circuits	
1850–	Transistors, Germanium PNP	
1851–	Transistors, Germanium NPN	
1853–	Transistors, Silicon PNP	
1854–	Transistors, Silicon NPN	
1855–	Field-Effect Transistors	
1900– thru 1912–	Diodes	
1920– thru 1952–	Vacuum Tubes	
1990–	Semiconductor Photosensitive and Light-Emitting Diodes	
3100– thru 3106–	Switches	
8120–	Cables	
9100–	Transformer, Coils, Chokes, Inductors, and Filters	

5-10. For example, 1854–0037, 1854–0221, and 1851–0192 are all NPN transitors. The first two are silicon and the last is germanium.

5-11. General Usage Parts

5-12. The following list gives the prefixes for HP manufactured parts used in several instruments, e.g., side frames, feet, top and bottom covers, etc. These are eight-digit part numbers with the four-digit prefix identifying the type of parts as shown below:

Type of Part	Prefix
Sheet Metal	5000– to 5019–
Machined	5020– to 5039–
Molded	5040– to 5059–
Assemblies	5060– to 5079–
Components	5080– to 5099–

5-13. Specific Instrument Parts

5-14. These are HP manufactured parts for use in individual instruments or series of instruments. For these parts, the prefix indicates the instrument and the suffix indicates the type of part. For example, 05036-60001 is an assembly used in the 5036A. Following is a list of suffixes commonly used.

Type of Part	P/N Suffix
Sheet Metal	-00000 to -00499
Machined	-20000 to -20499
Molded	-40000 to -40499
Assembly	-60000 to -60499
Component	-80000 to -80299
Documentation	-90000 to -90249

Table 5-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05036-60001	5	1	MICROPROCESSOR ASSEMBLY	28480	05036-60001
A1C1	0160-4554	7	11	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C2	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C4	0180-0210	6	2	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A1C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C7	0180-1746	5	3	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C10	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C12	0180-0210	6		CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A1C13	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1CR1	1901-0518	8	1	DIODE-SCHOTTKY	28480	1901-0518
A1CR2	1901-0731	7	1	DIODE-PWR RECT 400V 1A	28480	1901-0731
A1DS1	1990-0652	8	7	LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	HLMP-6620(1X4)
A1DS2	1990-0652	8		LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	HLMP-6620(1X4)
A1DS3	1990-0652	8		LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	HLMP-6620(1X4)
A1DS4	1990-0652	8		LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	HLMP-6620(1X4)
A1DS5	1990-0652	8		LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	HLMP-6620(1X4)
A1DS6	1990-0652	8		LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	HLMP-6620(1X4)
A1DS7A	1990-0685	7	2	LED-VISIBLE LUM-INT=0.2MCD MIN	28480	1990-0685
A1DS7B	1990-0685	7		LED-VISIBLE LUM-INT=0.2MCD MIN	28480	1990-0685
A1DS8	1990-0652	8		LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	HLMP-6620(1X4)
A1DS9	1990-0667	5	3	LED-VISIBLE 2 CHAR. 0.53IN. 2MA MAX	28480	1990-0667
A1DS10	1990-0667	5		LED-VISIBLE 2 CHAR. 0.53IN. 2MA-MAX	28480	1990-0667
A1DS11	1990-0667	5		LED-VISIBLE 2 CHAR. 0.53IN. 2MA-MAX	28480	1990-0667
A1DS12	1990-0673	3	2	LED-VISIBLE LUM-INT=1.5MCD IF=20MA-MAX	28480	5082-4690
A1DS13	1990-0675	5	4	LED-VISIBLE LUM-INT=1.5MCD IF=20MA-MAX	28480	5082-4590
A1DS14	1990-0674	4	2	LED-VISIBLE LUM-INT=2MCD IF=30MA-MAX	28480	5082-4990
A1DS15	1990-0675	5		LED-VISIBLE LUM-INT=1.5MCD IF=20MA-MAX	28480	5082-4590
A1DS16	1990-0673	3		LED-VISIBLE LUM-INT=1.5MCD IF=20MA-MAX	28480	5082-4690
A1DS17	1990-0675	5		LED-VISIBLE LUM-INT=1.5MCD IF=20MA-MAX	28480	5082-4590
A1DS18	1990-0674	4		LED-VISIBLE LUM-INT=2MCD IF=30MA-MAX	28480	5082-4990
A1DS19	1990-0675	5		LED-VISIBLE LUM-INT=1.5MCD IF=20MA-MAX	28480	5082-4590
A1LS1	9160-0246	5	1		28480	9160-0246
A1R1	1810-0280	8	3	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	11236	750-101-R10K
A1R2	0757-0401	0	3	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R3	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R4	1810-0382	1	1	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	28480	1810-0382
A1R5	1810-0280	8		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	11236	750-101-R10K
A1R6	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R7	1810-0273	9	1	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	11236	750-101-R470
A1R8	1810-0280	8		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	11236	750-101-R10K
A1S1	3101-1856	5	2	SWITCH-SL 8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
A1S2	3101-2363	1	1		28480	3101-2363
A1S3	3101-1856	5		SWITCH-SL 8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
A1S4- A1S29	5060-9436	7	26	SWITCH, PUSHBUTTON MOM.	28480	5060-9436
A1U1	1820-1794	2	3	IC BFR TTL LS NON-INV OCTL	27014	DM81LS95N
A1U2	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	SN74LS374PC
A1U3	1820-2074	3	1	IC MICPROC NMOS 8-BIT	34649	P8085
A1U4	1818-0773	6	1	IC NMOS 16384-BIT PROM 450-NS 3-S	28480	1818-0773
A1U5	1818-0438	4	2	IC NMOS 4K RAM STAT 450-NS 3-S	34649	P2114
A1U6	1818-0438	4		IC NMOS 4K RAM STAT 450-NS 3-S	34649	P2114
A1U7	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U8	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A1U9	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U10	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A1U11	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U12	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A1U13	1820-1794	2		IC BFR TTL LS NON-INV OCTL	27014	DM81LS95N
A1U14	1820-1794	2		IC BFR TTL LS NON-INV OCTL	27014	DM81LS95N
A1U15	1820-1730	6	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U16	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U17	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U18	1820-1759	9	1	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A1U19	1820-2138	0	1	IC DRVR MOS* DSPL DRVR OCTL	27014	DS8871N
A1U20	1820-1231	2	1	IC DRVR MOS HEX 1-INP	01295	SN75492N

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1W1- A1W14	1258-0124	7	14	PIN, PROGRAMMING JUMPER	91506	8136-475G1
A1XU4	1200-0475	7	1	SOCKET-IC MINISERT	28480	1200-0475
A1Y1	0410-1142	4	1	CRYSTA, QUARTZ	28480	0410-1142
				A1 MISCELLANEOUS PARTS		
	1390-0099	5	1	FASTENER-SNAP-IN PLGR PANEL THKNS	28480	1390-0099
	1390-0104	3	1	FASTENER-SNAP-IN GROM PANEL THKNS	28480	1390-0104
	1390-0462	6	2		28480	1390-0462
	5041-0829	4		KEY #1	28480	5041-0829
	5041-0830	7		KEY #2	28480	5041-0830
	5041-0831	8		KEY #3	28480	5041-0831
	5041-0832	9		KEY #4	28480	5041-0832
	5041-0833	0		KEY #5	28480	5041-0833
	5041-0834	1	2	KEY #6	28480	5041-0834
	5041-0835	2	1	KEY #7	28480	5041-0835
	5041-0836	3	1	KEY #8	28480	5041-0836
	5041-0838	5	1	KEY #0	28480	5041-0838
	5041-1673	8	1	KEY, FULL A	28480	5041-1673
	5041-1674	9	1	KEY, FULL B	28480	5041-1674
	5041-1675	0	1	KEY, FULL C	28480	5041-1675
	5041-1676	1	1	KEY, FULL D	28480	5041-1676
	5041-1677	2	1	KEY, FULL E	28480	5041-1677
	5041-1678	3	1	KEY, FULL F	28480	5041-1678
	5041-1679	4	1	KEY, FULL RESET	28480	5041-1679
	5041-1680	7	1	KEY, FULL DECODER	28480	5041-1680
	5041-1681	8	1	KEY, RUN K=0229 N	28480	5041-1681
	5041-1683	0	1	KEY, PC FETCH K=0229 N	28480	5041-1683
	5041-1684	1	1	KEY, ADDRESS, FETCH, K=0229 N	28480	5041-1684
	5041-1685	2	1	KEY, STEP, INSTRUMENT, K=0229 N	28480	5041-1685
	5041-1686	3	1	KEY, STEP, HARDWARE, K=0229 N	28480	5041-1686
	5041-1687	4	1	KEY, STORE/INCR, K=0229 N	28480	5041-1687
	5041-1688	5	1	KEY, INTERPRET, K=0229 N	28480	5041-1688
	5041-1689	6	1	KEY, REG. FETCH, K=0229 N	28480	5041-1689
A2	05036-60002	6	1	POWER SUPPLY ASSEMBLY (SERIES 1812)	28480	05036-60002
A2C1	0180-0567	6	1	CAPACITOR-FXD 8000UF+75-10% 30VDC AL	00853	500802U030A828
A2C2	0180-0117	2	4	CAPACITOR-FXD 2.7UF+-10% 35VDC TA	56289	150D275X9035B2
A2C3	0180-0117	2		CAPACITOR-FXD 2.7UF+-10% 35VDC TA	56289	150D275X9035B2
A2C4	0180-0117	2		CAPACITOR-FXD 2.7UF+-10% 35VDC TA	56289	150D275X9035B2
A2C5	0180-0117	2		CAPACITOR-FXD 2.7UF+-10% 35VDC TA	56289	150D275X9035B2
A2CR1	1901-0662	3	2	DIODE-PWR RECT 100V 6A	04713	MR751
A2CR2	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A2S1	3101-2046	7	1	SWITCH-SL DPDT-NS STD 1.5A 250VAC PC	28480	3101-2046
A2S2	3101-0693	6	1	SWITCH-SL 2-DPDT-NS STD 1.5A 250VAC PC	28480	3101-0693
A2U1	1826-0122	0	2	IC 7805 V RGLTR TO-220	07263	7805UC
A2U2	1826-0122	0		IC 7805 V RGLTR TO-220	07263	7805UC
				CHASSIS PARTS		
F1	2110-0004	1	1	FUSE .25A 250V FAST-BLO 1.25X.25 UL IEC	28480	2110-0004
F1	2110-0012	1	1	FUSE .5A 250V FAST-BLO 1.25X.25 UL IEC	28480	2110-0012
J1	1251-2357	8	1	CONNECTOR-AC PWR HP-9 MALE FLG-MTG	28480	1251-2357
T1	9100-4088	5	1	TRANSFORMER, POWER	28480	9100-4088
				MISCELLANEOUS PARTS		
	0362-0187	2	1	TUBING-HS .5-D/.25-RCVD .04-WALL POLYO	28480	0362-0187
	0510-0640	7	2		28480	0510-0640
	1400-0249	0	2	CABLE TIE .062-.625-DIA .091-WD NYL	28480	1400-0249
	1540-0537	5	1		28480	1540-0537
	2110-0565	9	1	FUSEHOLDER CAP BAYONET; 12A, 250V MAX	28480	2110-0565
	2110-0566	0	1	FUSEHOLDER-EXTR POST 12A 250V	28480	2110-0566
	8120-1378	1	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT	28480	8120-1378
	05036-00001	9	1	COVER, POWER SUPPLY (TOP)	28480	05036-00001
	05036-00002	0	1	COVER, POWER SUPPLY (BOTTOM)	28480	05036-00002
	9223-0473			STRAP, SETUP	28480	9223-0473

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-2. Manufacturers Code List

Mfr No.	Name	Address	Zip Code
00853	SANGAMO ELEC CO S CAROLINA DIV	PICKENS, SC	29671
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS, TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX, AZ	85062
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW, CA	94042
11236	CTS OF BERNE INC	BERNE, IN	46711
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD, PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA, CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO, CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE, CA	94086
34649	INTEL CORP	MOUNTAIN VIEW, CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS, MA	01247
91506	AUGAT INC	ATTLEBORO, MA	02703

SECTION VI
MANUAL CHANGES

6-1. INTRODUCTION

6-2. This section normally contains information for adapting this manual to instruments for which the content does not apply directly. Since this manual does apply directly to instruments having serial numbers listed on the title page, no change information is given here. Refer to INSTRUMENTS COVERED BY MANUAL in Section I for additional important information about serial number coverage.

SECTION VII
SERVICE

7-1. INTRODUCTION

7-2. This section provides safety considerations, disassembly and reassembly, troubleshooting procedures, component location photos, and schematic diagram (service information).

7-3. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

7-4. *Figure 7-1* shows symbols, reference designation and printed circuit board identification.

7-5. SAFETY CONSIDERATIONS

7-6. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by qualified service personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR (INSIDE OR OUTSIDE THE INSTRUMENT) OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE INSTRUMENT DANGEROUS. INTENTIONAL INTERRUPTION IS PROHIBITED.

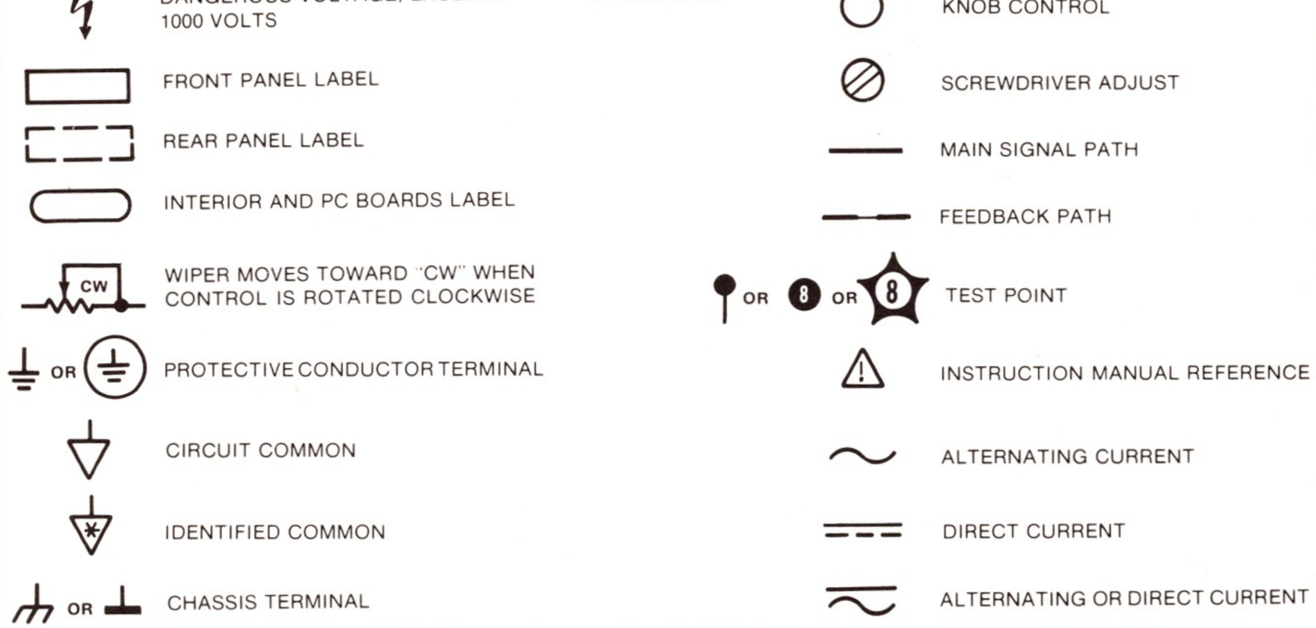
7-7. Any adjustment, maintenance, and repair of the opened power supply under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

7-8. Capacitors inside the power suppy may still be charged even if the instrument has been disconnected from its source of supply.

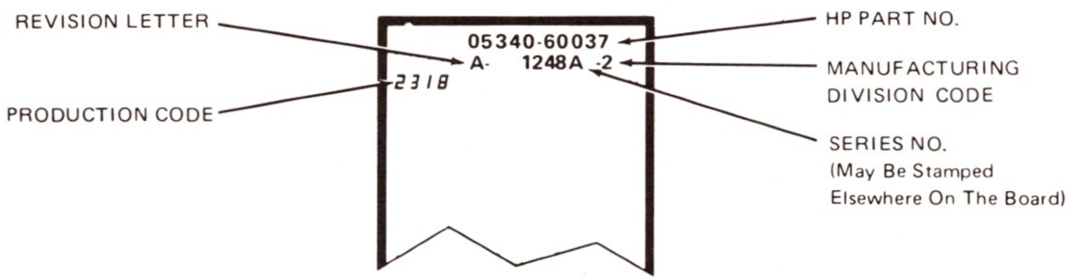
7-9. Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

7-10. Whenever it is likely that this protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

SYMBOLS



PRINTED CIRCUIT BOARD IDENTIFICATION



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

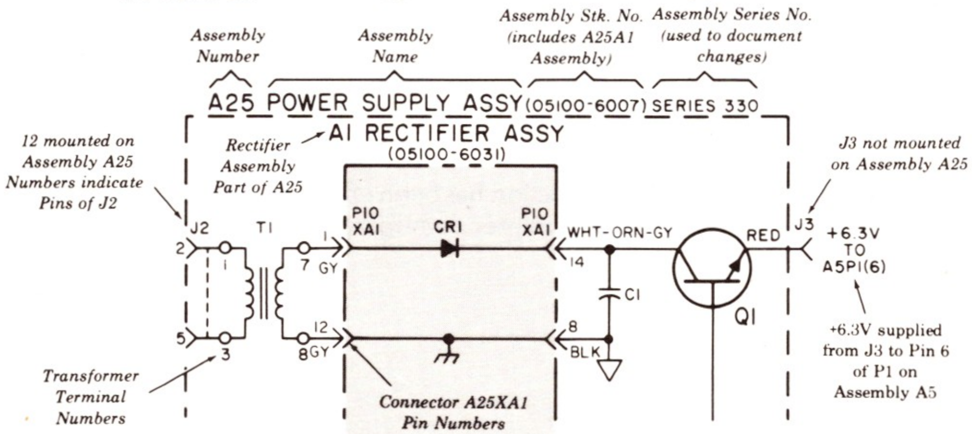


Figure 7-1. Schematic Diagrams Notes

7-11. DISASSEMBLY AND REASSEMBLY

7-12. Perform the following steps prior to disassembly or reassembly of the instrument.

a. Set LINE ON-OFF switch to OFF position.

b. Remove line power cable from Power Supply connector.

7-13. A1 Microprocessor Assembly Removal

7-14. Remove A1 Assembly as follows:

a. Loosen two screws at either the top or bottom hinge and lift A1 upward within limits of the power supply cord.

b. To remove A1 completely, unsolder power supply cord connections to A1 and clip the cable tie.

7-15. Power Supply Removal

7-16. Remove power supply as follows:

a. Remove A1 assembly as described in paragraph 7-14.

b. Loosen two screws at each end and at back of case (outside).

c. Remove two screws at top of inner liner and lift liner upward.

d. Remove power supply chassis by removing two front handle attaching screws from inside top front of case. Lift chassis upward.

e. To gain access to power supply parts, remove two screws at side and at end of power supply chassis and remove cover.

f. To remove A2 Power Supply PC Assembly, remove attaching screws and standoffs. Remove nuts that attach voltage regulators U1 and U2. Disconnect attaching wires if board is to be completely separated.

7-17. Reassembly

7-18. Reassembly procedures are essentially the reverse of disassembly.

7-19. TROUBLESHOOTING

7-20. This troubleshooting section consists of three main parts: recommended troubleshooting equipment, general troubleshooting procedures, and detailed signature analysis. For more extensive basic microprocessor troubleshooting information, refer to Chapter 5 in the "Practical Microprocessors" textbook.

7-21. The operation and use of recommended test equipment is described below, followed by an overall troubleshooting procedure. Next, a detailed method is shown for performing signature analysis in a test loop mode, or alternately, in a freerun mode of operation.

7-22. TROUBLESHOOTING EQUIPMENT

7-23. The instruments listed in *Table 1-3* are described in the following paragraphs and are recommended for troubleshooting the 5036A. Operating and service information for these instruments is contained in the manual supplied with each instrument.

7-24. HP 5004A Signature Analyzer

7-25. The HP 5004A Signature Analyzer provides a convenient means of very accurately identifying faulty logic nodes. The HP 5004A can convert the complex serial data stream present on a microprocessor circuit logic node into a four-digit "signature". To use signature anlaysis, the product under test must be designed to accommodate it, as is the 5036A. This section of the manual provides signature listings and test setup information. Circuits in the suspected area of the fault are probed until a signature is found which does not agree with the listing. The signal path is then traced backwards until a correct signature is found, localizing the fault.

7-26. HP 545A Logic Probe, HP 546A Logic Pulser, and HP 547A Current Tracer

7-27. The Logic Probe, Logic Pulser, and Current Tracer are self-contained troubleshooting instruments designed to stimulate and measure digital activity in logic circuits. When bad signatrues on the 5004A indicate printed circuit opens or shorts in the 5036A circuits, these three instruments are very effective in isolating the specific point.

7-28. The Logic Probe is a self-contained, easy-to-use tool for examining logic nodes. Continuity, signal flow, bus device, address decoder, clock, and switch activity of the 5036A may be verified. The circuits operating characteristics while in the hardware single step mode may be examined.

7-29. The Logic Pulser forces overriding pulses into logic nodes. It can be programmed to output single pulses, pulse streams, or bursts. The pulser can be used to force ICs to enable or clock. When used with the Logic Probe, logic circuit inputs can be pulsed while their outputs are monitored with the probe. By this means, correct signal propagation through logic elements can be verified.

7-30. The Current Tracer can be used to monitor current activity on a logic node or power bus and can tell approximately how much pulse current is present and what path it takes. When a Logic Pulser is used to inject current into a nonactive (no pulse activity) node, the impedance and the nature of possible stuck nodes (e.g., output, hard short) can be estimated. Then the actual low impedance point can be found by tracing the path of the current from the Logic Pulser to the location where the current either goes to a short or enters a component.

NOTE

Figure 7-6 shows the traces on the top and bottom of the pc board as an aid in signal tracing.

7-31. TROUBLESHOOTING PROCEDURES

7-32. Basic troubleshooting procedures for the 5036A are shown in the troubleshooting flowchart, *Figure 7-2*. Detailed procedures that correspond to the flowchart are described in the following paragraphs. After becoming familiar with the detailed procedures, use the abbreviated procedures, paragraph 7-71.

7-33. When a trouble is indicated in the 5036A's operation, the position of the fault jumper-plugs should be checked. These jumper-plugs are used to insert typical faults for training purposes. The positions of these jumper-plugs for normal operation are shown by dots on the back of the board under the correct jumper positions.

7-34. To start the troubleshooting procedure, turn on the 5036A power and observe the display for uLAb UP . If display indicates IC4 , IC5 or IC6 , check the IC indicated. If display does not appear, observe the bus and status LEDs. If not lit, check the power

supply. If lit, check for bus activity with the Logic Probe. If there is no bus activity check the control lines of microprocessor U3 for the logic levels that indicate the microprocessor is running, as follows:

Reset — Pin 36 High
Hold — Pin 39 Low
Clock — Pin 37 Flashing
Ready — Pin 35 High

7-35. If there is bus activity, refer to SIGNATURE ANALYSIS, paragraph 7-36.

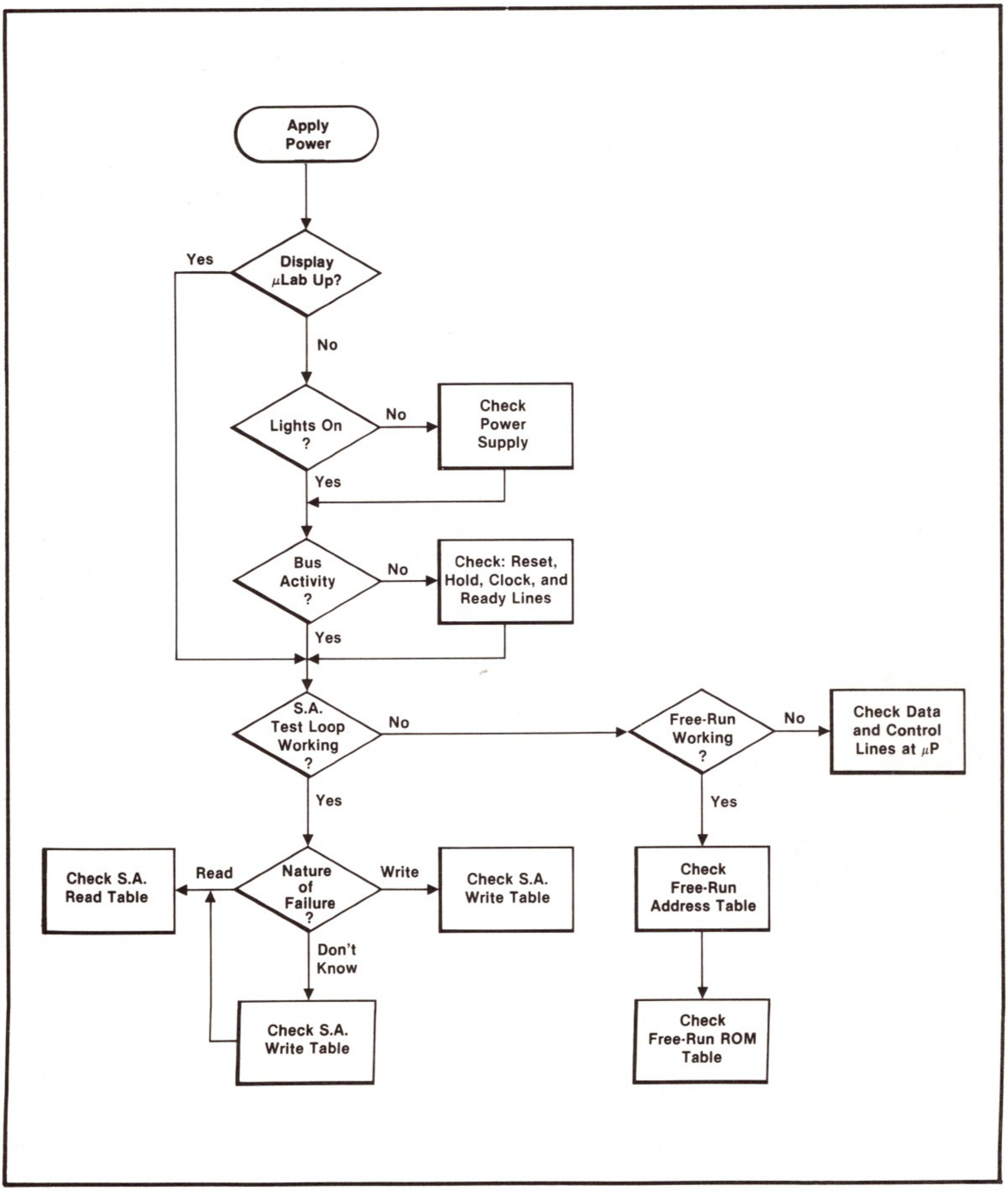


Figure 7-2. Troubleshooting Flowchart

7-36. SIGNATURE ANALYSIS

7-37. Signature Analysis (SA) provides a convenient method to isolate trouble in microprocessor circuits. The 5004A Signature Analyzer converts the logic activity at a circuit node into a four-digit "signature". This section of the manual includes listings (tables) of the signatures to be found at all important points in the 5036A circuit. To troubleshoot the circuit, the suspected points are probed until a signature is found which does not agree with the listing. The signal path is then traced backwards until a correct signature is found, and the fault is now localized.

7-38. The 5004A test pod requires three connections (plus ground) in addition to the probe: START, STOP, and CLOCK. The CLOCK signal synchronizes the two instruments. The START and STOP signals control the period of time of the measurement. The signature tables in this manual specify where to make connections. The connection points are shown in *Figure 7-3*. A typical test setup is shown in *Figure 7-4*.

7-39. In order to get meaningful signatures, a special program in ROM exercises the entire system to as great an extent as possible. This program is referred to as the SA Test Loop. When this program runs, the main part of the system is operating. The SA Test Loop detailed description and procedures are contained in paragraphs 7-46 through 7-54. The only problem with this test scheme is that the microprocessor must be capable of running the test loop. If a fault exists which prevents the microprocessor from running at all, then the test loop cannot operate. The solution is to "freerun" the processor. This is done by disconnecting the data bus from the processor (by means of the BUS switch) and forcing a NO OP instruction into the processor. The processor will read and execute this instruction and then increment its address lines. Then it will read the instruction again, and increment its address lines, and this will repeat indefinitely. This has the effect of incrementing the address lines repeatedly through all of the address space, which will exercise the decoders, the ROM and other portions of the circuit. The decoders and the memories do not need to be functional for this to work. Only the processor itself and its immediate circuitry must work. So even if the processor refuses to freerun, the problem has been narrowed down significantly. The freerun test detailed description and procedures are contained in paragraphs 7-55 through 7-70.

7-40. 5036A Test Modes

7-41. There are four SA test modes for the 5036A as follows: SA Write, SA Read, Freerun Address, and Freerun ROM. The troubleshooting flowchart in *Figure 7-2* provides a guide as to which mode to use. If the SA Test Loop (described in paragraph 7-46) will run, use it. There are two different clock connections for the SA Test Loop, READ and WRITE (see *Figure 7-3*). If the problem is write related (can't write to the output port or display), use the WRITE connection. If the problem is read related (can't read the input port or keyboard), then use the READ connection. If it's not evident whether a READ or WRITE problem exists or if the problem exists for both modes, use either connection and then switch if no bad signatures are found.

7-42. If the SA Test Loop (described in paragraph 7-46) will not run, the Freerun mode (described in paragraph 7-55) must be used. The two sets of connections on the 5036A boards for this mode are "ROM" and "A15". See *Figure 7-4*. The ROM connection is used to verify the ROM by taking signatures off the data lines, while the A15 address connection is used for general troubleshooting.

7-43. Signature Tables

7-44. There are four signature tables, each covering one test mode (*Tables 7-1* through *7-4*). At the beginning of each table, the START, STOP, and CLOCK connections are specified. In addition, the V_{CC} (+5V) signature is listed which will enable verification of the correct connections. Note that if the fault affects the signals being used for START, STOP, or CLOCK, the V_{CC} signature (and all the other signatures in that section) will be wrong and a different test mode must be used.

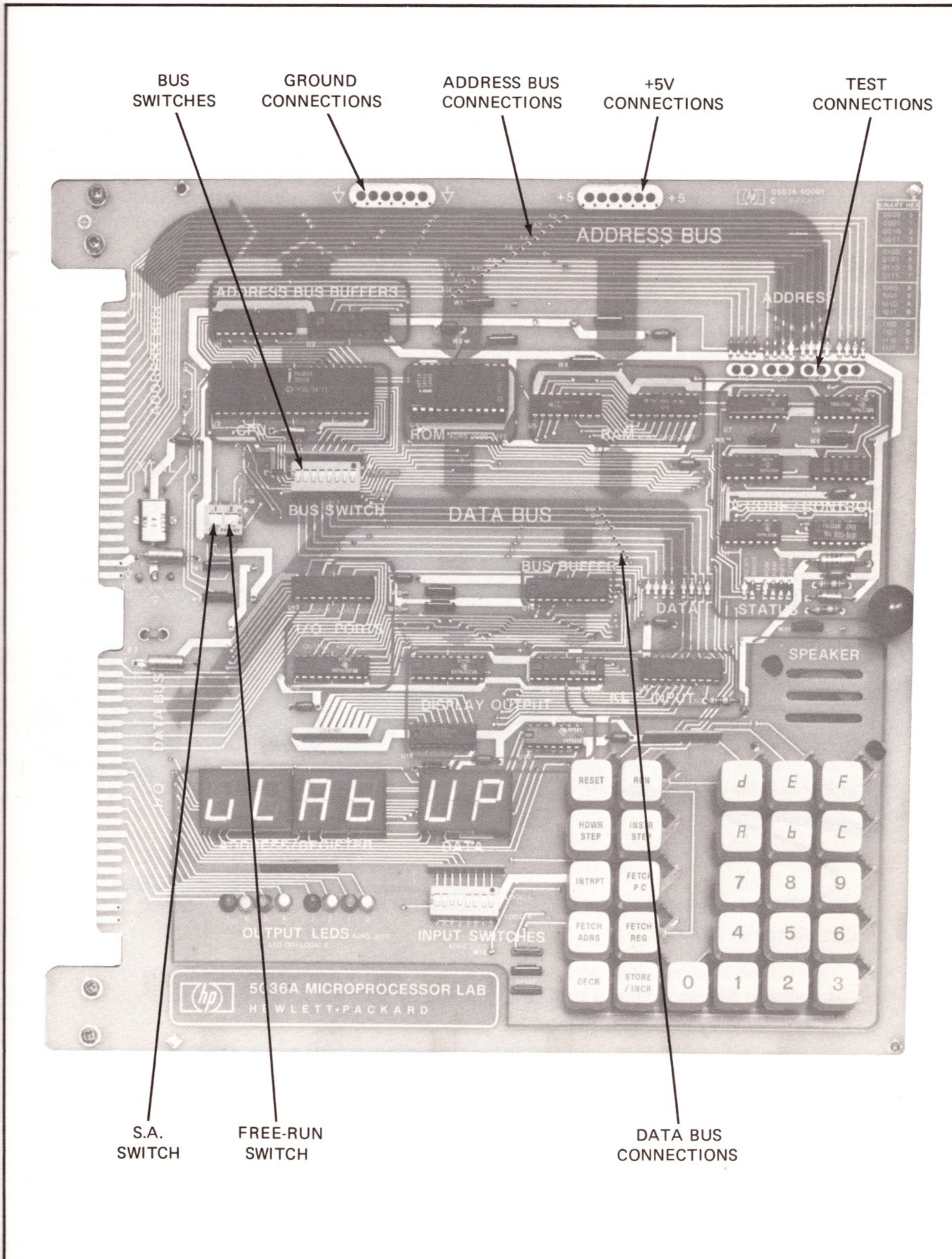


Figure 7-3. Test Switches and Connection Points

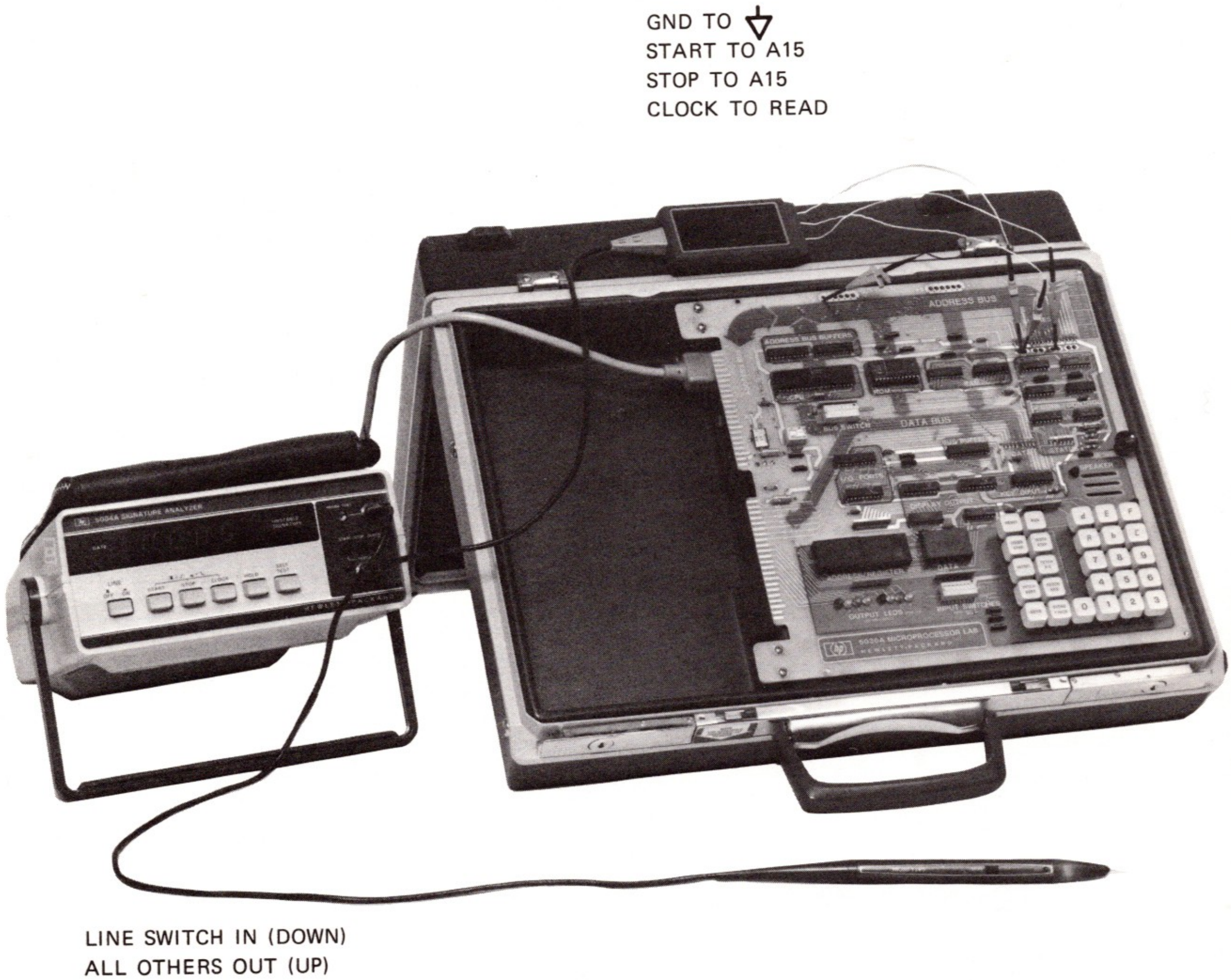


Figure 7-4. Typical Test Setup

7-45. The tables list every IC pin plus the address and data bus lines. In many cases a signature itself will be listed for the pin, but there are a number of different ways in which the signature may be represented. If the pin is tied directly to ground or +5V, the list will simply indicate GND or V_{CC} rather than giving the signature. The V_{CC} signature is listed at the beginning of the section, and the GND signature is always ØØØØ. The list may also show a 1 or Ø, which means the same thing as V_{CC} or GND except that the signal is a gate output, not tied directly to V_{CC} or GND. Finally, the list may show a 1B or ØB, which means the same thing as a 1 or Ø except that the light on the Signature Analyzer's probe tip should be blinking. This means that although the signal is always at the same level when the clock edge arrives, at other times it is at a different level.

7-46. SA Test Loop Description

7-47. This procedure is basically a half-split troubleshooting technique. The signature analysis test loop exercises more of the circuit than the freerun mode. Put the 5036A into the SA test loop by pressing RESET and then sliding the SA switch up and down once. All of the output LEDs and display segments should light and the speaker should beep once. Also, pressing the INTRPT key causes the speaker to beep repeatedly. If these actions occur, the SA loop is probably running. The best way to be sure is to connect the Signature Analyzer to the 5036A and check the V_{CC}(+5V) setup signature specified in *Table 7-1* or *7-2*. If the signature is correct, the SA Loop is running.

7-48. When the SA test loop runs, the essential portions of the system are operating satisfactorily. The microprocessor is addressing the ROM, is receiving instructions from the ROM through the data bus, and is executing these instructions.

7-49. There are two stimulus programs in the SA test loop. One program sends (writes) stimulus data patterns to the devices that the microprocessor talks to. The other program receives (reads) data from the devices that the microprocessor listens to. Both of these programs run alternately while in the SA test loop. By changing the connections to the Signature Analyzer, talk or listen devices can be checked.

7-50. The symptoms of the fault often point to a general portion of the circuit and are classified as a read or a write type of problem. For example, a bad display would most likely be a write problem. The Signature Analyzer is then connected according to the setup specified in the SA write loop table (*Table 7-1*). Signatures on nodes in the display circuit are then checked against entries in that table.

7-51. SA Write Test Procedure

7-52. To take signatures in the SA Write Test Loop, proceed as follows:

b. Connect the 5004A START and STOP leads to the 5036A A15 test slot. Connect the CLOCK lead to the WRITE test slot. Be sure the GND lead is still connected to ground.

a. Touch the Data Probe of the 5004A to any of the OUTPUT LED signal lines. Observe that the blinking tip shows pulse activity when the LEDs appear to be fully on. The reason for this activity, is that the LEDs are being turned off occasionally so that both output logic states of Out Port U15 can be checked when a signature is taken.

c. Set START, STOP, and CLOCK inputs on the 5004A to rising edges. The A15 bit is controlled by the SA Test Loop program and pulses high one time for each loop cycle. By clocking off of the WRITE line, the 5004A looks at data every time a write or output operation occurs.

d. Refer to *Table 7-1* and verify the setup by checking the V_{CC} signature.

e. Using *Table 7-1* check signatures on any nodes of interest. Note that input devices (using READ signal) are not checked in this SA test mode.

f. If trouble is not found, proceed to paragraph 7-53.

7-53. SA Read Test Procedure

7-54. To take signatures in the SA Read Test Loop, proceed as follows:

a. Connect the 5004A CLOCK lead to the READ slot on the 5036A. Signatures now will relate to devices that "talk to" the microprocessor.

b. Verify the test setup by touching the Data Probe tip to V_{CC} and checking the signature in *Table 7-2*. This setup has the same set of connections and edge settings as the freerun address mode. The difference (and the reason why the V_{CC} signatures are different) is that in the freerun case A15 defined a cycle of 64K incrementing address cycles, whereas in the SA Test Loop, the software (program) is controlling the A15 line for use as a START and STOP control. The window length in this case is much less than 64K cycles because the test loop is much shorter.

c. Slide all of the INPUT switches down and check the signatures on the data bus lines against the entires in *Table 7-2*. They should agree.

d. Sliding the switches up should cause the signatures to change (line-by-line) until they agree with those in the table. These two steps demonstrate that the input switches are being read correctly on the data bus. Return them all to the down position.

e. Refer again to *Table 7-2* and verify the keyboard switches specified (avoid the RESET key) by pressing them and observing the corresponding data line.

f. The INTRPT key is tested by pressing it while in the SA Test Loop. It should cause the speaker to beep repeatedly.

g. Press RESET key twice to return the 5036A to its normal mode of operation.

7-55. Freerun Test Description

7-56. When the SA test loop won't run, the Freerun test mode is used to test smaller parts of the circuit. Opening the data bus lines to the microprocessor (slide the 8 BUS SWITCHES up) and inserting a freerun instruction (slide the FR switch up) causes the microprocessor to cycle through the address field on its own. Opening the data bus lines allows isolation of the microprocessor from the data bus and the rest of the system. In freerun, the microprocessor stimulates other portions of the circuit through the address bus. This address bus stimulus is unsophisticated compared to the well controlled data patterns used in the SA test loop. However, freerun does exercise portions of the address bus drive, decoding, and control circuits, as well as the ROM. The advantage of this test mode is that little more than the microprocessor chip has to operate to use it.

7-57. The freerun test mode can be identified by the action of the bus and status LEDs on the 5036A. The fourteen least-significant (right-most) address bus LEDs should be flashing so fast

that they appear to be steadily lit. The A15 and A14 LEDs should appear to flash rapidly. The status LEDs should behave as follows: READ "on"; WRITE "off"; ROM, RAM, INPUT, and OUTPUT flashing. The Freerun test consists of an address test, paragraph 7-59, and a ROM test, paragraph 7-62.

7-58. If the microprocessor won't freerun, check the control lines going to it (reset, hold, ready, and interrupt) and the clock to see if one of these is the cause. Also, check the data bus pins of the microprocessor to see if it is getting the freerun instruction. If they all appear to be good, the microprocessor is probably bad.

7-59. Freerun Address Test Description

7-60. The freerun address mode exercises most of the address and control portions of the 5036A. *Table 7-3* shows the correct setup and signatures. A correct V_{CC} signature verifies the proper test setup and freerunning of the microprocessor.

7-61. When the 5036A is freerunning correctly, the address bus and much of the decoding and control circuits can be tested. The first signatures to look at are those on the address bus lines. They should all agree with the signatures in *Table 7-3.* Signatures on the device chip select pins, the address decoder (U7), the other control circuits, and the microprocessor (U3) control pins can then be taken. If all of these signatures are correct, then the address, decode, and control portions of the system are probably good. However, if other problems are indicated, check the remainder of the signatures in *Table 7-3.* If these signatures are all correct, suspect a bad device on the data bus and go on to the freerun ROM test mode.

7-62. Freerun ROM Test Description

7-63. The freerun ROM test mode requires different connections to the Signature Analyzer so that it only samples data when the ROM is being addressed. In this way the contents of the ROM can be verified and faulty data bus lines can be detected. Either of these conditions could prevent the 5036A from running the SA test program (or any other program).

7-64. The procedure for testing the ROM is to first connect the Signature Analyzer to the 5036A according to *Table 7-4* (while still in the freerun test mode). Verify the setup by checking the V_{CC} signature and then checking each of the eight data bus lines. A bad signature on any one of these lines should be checked at the corresponding ROM output pin to determine a ROM output versus a board trace problem. If bad signatures are found on all of the bus lines, the ROM enable and address signals should be checked at the ROM pins. If these signatures are good then another device may be erroneously enabled onto the data bus. This would create a bus conflict. Signatures on the other bus device enable pins can check for this. If they are good, the system can be stopped while the ROM is enabled. The Logic Pulser and Current Tracer can then be used to find the offending bus device.

7-65. Freerun Test Preliminary Procedures

7-66. Perform the following preliminary procedures prior to conducting the Freerun Address Test, paragraph 7-67, or the Freerun ROM Test, paragraph 7-69.

a. FREERUN. Apply power to the 5036A. Slide all 8 sections of the BUS SWITCH to the up position. There are now no data bus signals going between the microprocessor and the rest of the system. There is no feedback path from the data bus to the microprocessor and therefore no instructions being sent to it. It is free ro run "open loop".

b. Slide the FREERUN switch, located to the lower left of the BUS SWITCH to the up position. This hardwires the MOV A to A instruction code (7F) to the microprocessor whenever it performs a read operation. The MOV A to A instruction is essentially a "do nothing"

or NO OP instruction which has the desired effect of causing the microprocessor to execute this instruction (and only this instruction) repeatedly at every single address, and therefore increments the address bus lines through all possible addresses. Refer to Chapter 2 of the "Practical Microprocessors" textbook for programming information.

NOTE

Besides the microprocessor, there are only a few other circuits on the board that could prevent this freerun mode from occurring. This circuitry is in the control portion and, in conjunction with the microprocessor, is often referred to as the kernel. The kernel can be a fundamental partitioning point for fault isolation in a microprocessor based system. If freerun doesn't occur (step d), the problem has been narrowed down to a small portion of the overall system.

c. Observe the ADDRESS bus LEDs. The visibly flashing A15 and A14 LEDs and the dim A13 to AØ LEDs indicate that the 5036A is indeed continuously cycling through the full address field. Note also that the READ LED indicates that the microprocessor is spending a great deal of its time reading (the instruction 7F). The DATA BUS LEDs do not show a dominance to 7F because they are now isolated (via the BUS SWITCH) from the microprocessor inputs. The ROM, RAM, INPUT, and OUTPUT LEDs which appear to be flashing together are actually flashing in quick succession as the high order address lines ripple through the Address Decoder circuit (U7) that drives these LEDs.

7-67. Freerun Address Test Procedures

7-68. Perform the following procedures to take signatures in the Freerun Address mode:

a. Connect the 5004A test pod GND lead to the 5036A ground connection (at top of board) and connect the START and STOP leads to the A15 slot and the CLOCK lead to the READ slot.

b. Set START, STOP, and CLOCK switches on the 5004A to the rising edge position (pushbuttons out). The GATE indicator should now be flashing to indicate that a signature gathering "window" is occurring. The window, in this case, is from one rising edge of the A15 address bit to the next rising edge; the full 65K address field. Signal data is being input to the 5004A at every rising edge of the READ line, 65K times during each measurement interval or window.

c. Touch the Data Probe (which also acts as a Logic Probe) to ground. Observe that the signature is Ø Ø Ø Ø. This is the characteristic logic Ø signature for all possible test setups.

d. Touch the Data Probe to a V_{CC} line to take the V_{CC} signature. Observe the signature Ø Ø Ø 1. This is the characteristic logic 1 signature (only for this setup). Verify that this is true by changing the slope switch on the START or STOP inputs. The Ø Ø Ø 1 display thus indicates that the test setup is correct and that the kernel is freerunning as expected. Had this not been the case, it could be assumed that a fault in the kernel existed. This greatly reduces the amount of the circuitry in the 5036A that would need to be considered as possible fault areas.

e. Take signatures on address bus lines AØ to A15 and verify that they agree with the entries in *Table 7-3*. Correct signatures indicate that the microprocessor, Address Buffer U1, and Address Latch U2 are operating properly.

f. Check signatures on Address Decoder U7 and other IC's to verify proper operation.

g. If trouble is not found, proceed to next paragraph.

7-69. Freerun ROM Test Procedures

7-70. To take signatures in the Freerun ROM mode, perform the following procedures:

a. Connect the START and STOP connectors to the ROM slot. Set the START edge low (button in) and leave the STOP edge high (button out) on the 5004A. The measurement window now begins the first time the ROM is read (when the ROM enable line goes low at address Ø Ø Ø Ø) and ends after the last time the ROM is read (ROM enable goes high at address Ø 8 Ø Ø). Although this measurement window is only 2K, the microprocessor still runs in the 65K long freerun loop. This allows, however, only looking at data for the 2K of the loop that the ROM is enabled.

b. Touch the Data Probe to V_{CC} and verify from *Table 7-4* that the proper setup signature is present.

c. Verify that signatures on each of the 8 DATA BUS lines agree with the ones in the table. This verifies all 2K × 8 bits of the ROM.

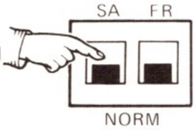
Table 7-1. S.A. Write Test

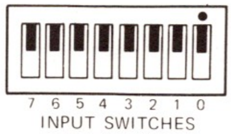
5004A SWITCHES		5036A CONNECTIONS
START	⌠	A15
STOP	⌠	A15
CLOCK	⌠	WRITE

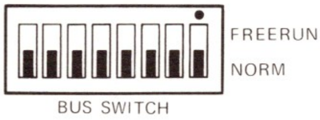
VCC SIGNATURE: 1CAU

5036A SWITCHES

MOVE UP
THEN DOWN







SIGNATURES

Data Lines		Address Lines			
D0	937H	A0	UU3P	A8	9P91
D1	C072	A1	209C	A9	0765
D2	F5A5	A2	HHCO	A10	0000-B
D3	UA0P	A3	85A9	A11	1P3H
D4	51H6	A4	6F64	A12	1C32
D5	AU8U	A5	7A21	A13	7A26
D6	2PPH	A6	A2UC	A14	0000-B
D7	H011	A7	3483	A15	9678

U1

Signature	Pin	Pin	Signature
GND	1	20	VCC
1P3H	2	19	0000
1P3H	3	18	9678
0000-B	4	17	9678
0000-B	5	16	0000-B
0765	6	15	0000-B
0765	7	14	7A26
9P91	8	13	7A26
9P91	9	12	1C32
GND	10	11	1C32

U2

Signature	Pin	Pin	Signature
0000	1	20	VCC
UU3P	2	19	3483
937H	3	18	H011
C072	4	17	2PPH
209C	5	16	A2UC
HHC0	6	15	7A21
F5A5	7	14	AU8U
UA0P	8	13	51H6
85A9	9	12	6F64
GND	10	11	1CAU-B

U3

Signature	Pin	Pin	Signature
X	1	40	VCC
X	2	39	0000
0000	3	38	0000
1CAU-B	4	37	1CAU-B
0000	5	36	1CAU
0000	6	35	1CAU
0000	7	34	FP05
0000	8	33	0000-B
0000	9	32	1CAU-B
0000	10	31	1CAU-B
1CAU	11	30	0000-B
937H	12	29	1CAU-B
C072	13	28	9678
F5A5	14	27	0000-B
UAOP	15	26	7A26
51H6	16	25	1C32
AU8U	17	24	1P3H
2PPH	18	23	0000-B
H011	19	22	0765
GND	20	21	9P91

U4

Signature	Pin	Pin	Signature
3483	1	24	VCC
A2UC	2	23	9P91
7A21	3	22	0765
6F64	4	21	1CAU
85A9	5	20	1CAU-B
HHC0	6	19	0000-B
209C	7	18	1CAU-B
UU3P	8	17	H011
937H	9	16	2PPH
C072	10	15	AU8U
F5A5	11	14	51H6
GND	12	13	UA0P

U5

Signature	Pin	Pin	Signature
A2UC	1	18	VCC
7A21	2	17	3483
6F64	3	16	9P91
85A9	4	15	0765
UU3P	5	14	937H
209C	6	13	C072
HHC0	7	12	F5A5
1FFA	8	11	UA0P
GND	9	10	0000-B

U6

Signature	Pin	Pin	Signature
A2UC	1	18	VCC
7A21	2	17	3483
6F64	3	16	9P91
85A9	4	15	0765
UU3P	5	14	51H6
209C	6	13	AU8U
HHC0	7	12	2PPH
1FFA	8	11	H011
GND	9	10	0000-B

U7

Signature	Pin	Pin	Signature
1P3H	1	16	VCC
1C32	2	15	1CAU-B
7A26	3	14	FP05
0000-B	4	13	39U4
9678	5	12	1CAU-B
1CAU-B	6	11	1CAU-B
9377	7	10	58P0
GND	8	9	AA1P

U8

Signature	Pin	Pin	Signature
1CAU	1	16	VCC
0000	2	15	0000
1CAU	3	14	1CAU
GND	4	13	HHC0
UU3P	5	12	209C
0599	6	11	1CAU
1P36	7	10	0000
GND	8	9	39U4

X = Don't Care Signature B = Blinking GND or VCC Signature

Table 7-1. S.A. Write Test (Continued)

U9

Pin	Signature	Pin	Signature
1	1CAU	14	VCC
2	1CAU	13	9P91
3	0000	12	0765
4	0000-B	11	1FFH
5	1CAU-B	10	1FFH
6	1CAU-B	9	1CAU-B
7	GND	8	0762

U10

Pin	Signature	Pin	Signature
1	1CAU-B	14	VCC
2	VCC	13	0000
3	0000	12	VCC
4	0000	11	209C
5	1CAU	10	VCC
6	0000-B	9	0000
7	GND	8	1CAU

U11

Pin	Signature	Pin	Signature
1	FP05	14	VCC
2	CCA8	13	1CAU
3	1FFA	12	1CAU
4	0599	11	1CAU
5	0762	10	1CAU-B
6	A007	9	1CAU-B
7	GND	8	1CAU-B

U12

Pin	Signature	Pin	Signature
1	A007	14	VCC
2	CCA8	13	1CAU
3	0000-B	12	0000
4	1CAU-B	11	0000
5	1CAU	10	1CAU
6	0000	9	1CAU
7	GND	8	0000

U13

Pin	Signature	Pin	Signature
1	1CAU-B	20	VCC
2	1CAU	19	1CAU-B
3	937H	18	1CAU
4	1CAU	17	H011
5	C072	16	ICAU
6	1CAU	15	2PPH
7	F5A5	14	1CAU
8	1CAU	13	AU8U
9	UA0P	12	1CAU
10	GND	11	51H6

U14

Pin	Signature	Pin	Signature
1	GND	20	VCC
2	937H	19	GND
3	937H	18	H011
4	C072	17	H011
5	C072	16	2PPH
6	F5A5	15	2PPH
7	F5A5	14	AU8U
8	UA0P	13	AU8U
9	UA0P	12	51H6
10	GND	11	51H6

U15

Pin	Signature	Pin	Signature
1	VCC	20	VCC
2	HA59	19	CCC4
3	937H	18	H011
4	C072	17	2PPH
5	PH2F	16	7769
6	7696	15	PPH2
7	F5A5	14	AU8U
8	UA0P	13	51H6
9	CC4C	12	HHA5
10	GND	11	AA1P

U16

Pin	Signature	Pin	Signature
1	VCC	20	VCC
2	6PPH	19	22HH
3	937H	18	H011
4	C072	17	2PPH
5	C776	16	45CC
6	5CCC	15	8C77
7	F5A5	14	AU8U
8	UA0P	13	51H6
9	2HHH	12	16PP
10	GND	11	9377

U17

Pin	Signature	Pin	Signature
1	VCC	20	VCC
2	65CU	19	C15H
3	937H	18	H011
4	C072	17	2PPH
5	8957	16	70PP
6	A5A1	15	1625
7	F5A5	14	AU8U
8	UA0P	13	51H6
9	6037	12	81H5
10	GND	11	58P0

U18

Pin	Signature	Pin	Signature
1	0000	20	VCC
2	1CAU-B	19	1CAU-B
3	0000-B	18	1CAU
4	1CAU-B	17	UA0P
5	1CAU-B	16	1CAU
6	1CAU-B	15	F5A5
7	1CAU-B	14	1CAU
8	1CAU-B	13	C072
9	1CAU-B	12	1CAU
10	GND	11	937H

U19

Pin	Signature	Pin	Signature
1	6PPH	18	VCC
2	C776	17	X
3	5CCC	16	X
4	2HHH	15	X
5	16PP	14	X
6	8C77	13	X
7	45CC	12	X
8	22HH	11	X
9	X	10	X

U20

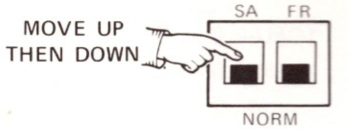
Pin	Signature	Pin	Signature
1	X	14	65CU
2	X	13	X
3	81H5	12	8957
4	GND	11	VCC
5	1625	10	A5A1
6	X	9	X
7	X	8	6037

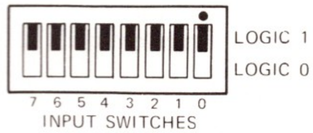
Table 7-2. S.A. Read Test

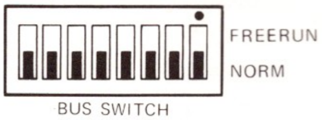
5004A SWITCHES	5036A CONNECTIONS
START ⌠	A15
STOP ⌠	A15
CLOCK ⌠	READ

VCC SIGNATURE: AU35

5036A SWITCHES







SIGNATURES

Data Lines		Address Lines			
D0	0122	A0	773F	A8	3U98
D1	A7FP	A1	4H2F	A9	3U98
D2	8863	A2	6087	A10	2UP0
D3	H3A4	A3	5HA7	A11	AAH3
D4	F616	A4	6757	A12	954C
D5	5C74	A5	HUC6	A13	52A9
D6	P165	A6	1C96	A14	0000-B
D7	36A9	A7	PAU5	A15	78AU

U1

Signature	Pin	Pin	Signature
GND	1	20	VCC
AAH3	2	19	0000
AAH3	3	18	78AU
2UP0	4	17	78AU
2UP0	5	16	0000-B
3U98	6	15	0000-B
3U98	7	14	52A9
3U98	8	13	52A9
3U98	9	12	954C
GND	10	11	954C

U2

Signature	Pin	Pin	Signature
0000	1	20	VCC
773F	2	19	PAU5
0122	3	18	36A9
A7FP	4	17	P165
4H2F	5	16	1C96
6087	6	15	HUC6
8863	7	14	5C74
H3A4	8	13	F616
5HA7	9	12	6757
GND	10	11	AU35-B

U3

Signature	Pin	Pin	Signature
X	1	40	VCC
X	2	39	0000
0000	3	38	0000
13F3	4	37	AU35-B
0000	5	36	AU35
0000	6	35	AU35
0000	7	34	CU4H
0000	8	33	AU35-B
0000	9	32	AU35-B
0000	10	31	AU35-B
AU35	11	30	0000-B
0122	12	29	2F69
A7FP	13	28	78AU
8863	14	27	0000-B
H3A4	15	26	52A9
F616	16	25	954C
5C74	17	24	AAH3
P165	18	23	2UP0
36A9	19	22	3U98
GND	20	21	3U98

U4

Signature	Pin	Pin	Signature
PAU5	1	24	VCC
1C96	2	23	3U98
HUC6	3	22	3U98
6757	4	21	AU35
5HA7	5	20	80H5
6087	6	19	2UP0
4H2F	7	18	0000-B
773F	8	17	36A9
0122	9	16	P165
A7FP	10	15	5C74
8863	11	14	F616
GND	12	13	H3A4

U5

Signature	Pin	Pin	Signature
1C96	1	18	VCC
HUC6	2	17	PAU5
6757	3	16	3U98
5HA7	4	15	3U98
773F	5	14	0122
4H2F	6	13	A7FP
6087	7	12	8863
90AH	8	11	H3A4
GND	9	10	AU35-B

U6

Signature	Pin	Pin	Signature
1C96	1	18	VCC
HUC6	2	17	PAU5
6757	3	16	3U98
5HA7	4	15	3U98
773F	5	14	F616
4H2F	6	13	5C74
6087	7	12	P165
90AH	8	11	36A9
GND	9	10	AU35-B

U7

Signature	Pin	Pin	Signature
AAH3	1	16	VCC
954C	2	15	80H5
52A9	3	14	90AH
0000-B	4	13	AU35
78AU	5	12	3A7P
AU35-B	6	11	UH9F
AU35-B	7	10	AU35-B
GND	8	9	AU35-B

U8

Signature	Pin	Pin	Signature
AU35	1	16	VCC
0000	2	15	0000
AU35	3	14	AU35
GND	4	13	6087
773F	5	12	4H2F
H443	6	11	AU35
7C76	7	10	0000
GND	8	9	AU35-B

X = Don't Care Signature   B = Blinking GND or VCC Signature

Table 7-2. S.A. Read Test (Continued)

U9

Signal	Pin	Pin	Signal
AU35	1	14	VCC
AU35	2	13	3U98
0000	3	12	3U98
AU35-B	4	11	90AH
0000-B	5	10	90AH
AU35-B	6	9	0000-B
GND	7	8	AU35-B

U10

Signal	Pin	Pin	Signal
AU35-B	1	14	VCC
VCC	2	13	0000
0000	3	12	VCC
0000	4	11	4H2F
AU35	5	10	VCC
0000-B	6	9	0000
GND	7	8	AU35

U11

Signal	Pin	Pin	Signal
90AH	1	14	VCC
0000-B	2	13	AU35
90AH	3	12	AU35
H443	4	11	AU35
AU35-B	5	10	0000-B
AU35-B	6	9	3A7P
GND	7	8	3A7P

U12

Signal	Pin	Pin	Signal
AU35-B	1	14	VCC
0000-B	2	13	AU35
0000-B	3	12	0000
AU35-B	4	11	0000
AU35	5	10	AU35
0000	6	9	AU35
GND	7	8	0000

U13

Signal	Pin	Pin	Signal
0000-B	1	20	VCC
AU35	2	19	UH9F
0122	3	18	AU35
AU35	4	17	36A9
A7FP	5	16	AU35
AU35	6	15	P165
8863	7	14	AU35
AU35	8	13	5C74
H3A4	9	12	AU35
GND	10	11	F616

U14

Signal	Pin	Pin	Signal
GND	1	20	VCC
0122	2	19	GND
0122	3	18	36A9
A7FP	4	17	36A9
A7FP	5	16	P165
8863	6	15	P165
8863	7	14	5C74
H3A4	8	13	5C74
H3A4	9	12	F616
GND	10	11	F616

U15

Signal	Pin	Pin	Signal
VCC	1	20	VCC
C202	2	19	0AF8
0122	3	18	36A9
A7FP	4	17	P165
H2F8	5	16	C214
674C	6	15	852F
8863	7	14	5C74
H3A4	8	13	F616
F19H	9	12	4C06
GND	10	11	AU35-B

U16

Signal	Pin	Pin	Signal
VCC	1	20	VCC
6C01	2	19	C139
0122	3	18	36A9
A7FP	4	17	P165
91AF	5	16	4P53
CA46	6	15	94F9
8863	7	14	5C74
H3A4	8	13	F616
92P9	9	12	324C
GND	10	11	AU35-B

U17

Signal	Pin	Pin	Signal
VCC	1	20	VCC
HF4A	2	19	4787
0122	3	18	36A9
A7FP	4	17	P165
7H76	5	16	882F
3011	6	15	P21H
8863	7	14	5C74
H3A4	8	13	F616
4923	9	12	H071
GND	10	11	AU35-B

U18

Signal	Pin	Pin	Signal
0000	1	20	VCC
AU35-B	2	19	3A7P
AU35-B	3	18	AU35
AU35-B	4	17	H3A4
0000-B	5	16	AU35
13F3	6	15	8863
13F3	7	14	AU35
13F3	8	13	A7FP
13F3	9	12	AU35
GND	10	11	0122

U19

Signal	Pin	Pin	Signal
6C01	1	18	VCC
91AF	2	17	X
CA46	3	16	X
92P9	4	15	X
324C	5	14	X
94F9	6	13	X
4P53	7	12	X
C139	8	11	X
X	9	10	X

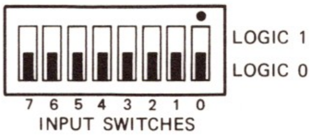
U20

Signal	Pin	Pin	Signal
X	1	14	HF4A
X	2	13	X
H071	3	12	7H76
GND	4	11	VCC
P21H	5	10	3011
X	6	9	X
X	7	8	4923

Table 7-2. S.A. Read Test (Continued)

NOTE

Place all INPUT SWITCHES down for the Input Port Test and Keyboard Test and check data line signatures as shown:



Input Port Test

D0	538C
D1	U567
D2	HAFA
D3	810H
D4	94CU
D5	09HH
D6	C3FF
D7	6400

Keyboard Test

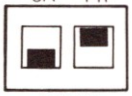
D0	F6F0	when 0, 1, 4, 7, A or d key is pressed
D1	602F	when 2, 5, 8, b or E key is pressed
D2	4U81	when 3, 6, 9, C or F key is pressed
D3	1446	when HDWR STEP key is pressed

Table 7-3. Freerun Address Test

5004A SWITCHES	5036A CONNECTIONS
START ⎍	A15
STOP ⎍	A15
CLOCK ⎍	READ

VCC SIGNATURE: 0001

5036A SWITCHES

SA FR

NORM

BUS SWITCH

INPUT SWITCHES

SIGNATURES

Data Lines		Address Lines			
D0	X	A0	UUUU	A8	HC89
D1	X	A1	5555	A9	2H70
D2	X	A2	CCCC	A10	HPP0
D3	X	A3	7F7F	A11	1293
D4	X	A4	5H21	A12	HAP7
D5	X	A5	0AFA	A13	3C96
D6	X	A6	UPFH	A14	3827
D7	X	A7	52F8	A15	755P

U1

GND	1	20	VCC
1293	2	19	0000
1293	3	18	755P
HPP0	4	17	755P
HPP0	5	16	3827
2H70	6	15	3827
2H70	7	14	3C96
HC89	8	13	3C96
HC89	9	12	HAP7
GND	10	11	HAP7

U2

0000	1	20	VCC
UUUU	2	19	52F8
0001-B	3	18	0000-B
0001-B	4	17	0001-B
5555	5	16	UPFH
CCCC	6	15	0AFA
0001-B	7	14	0001-B
0001-B	8	13	0001-B
7F7F	9	12	5H21
GND	10	11	0001-B

U3

X	1	40	VCC
X	2	39	0000
0000	3	38	0000
0000 or 0001	4	37	0001-B
0000	5	36	0001
0000	6	35	0001
0000	7	34	0000
0000	8	33	0001
0000	9	32	0001-B
0000	10	31	0001
0001	11	30	0000-B
0001-B	12	29	0001
0001-B	13	28	755P
0001-B	14	27	3827
0001-B	15	26	3C96
0001-B	16	25	HAP7
0001-B	17	24	1293
0001-B	18	23	HPP0
0000-B	19	22	2H70
GND	20	21	HC89

U4

52F8	1	24	VCC
UPFH	2	23	HC89
0AFA	3	22	2H70
5H21	4	21	0001
7F7F	5	20	3PCF
CCCC	6	19	HPP0
5555	7	18	0000-B
UUUU	8	17	X
X	9	16	X
X	10	15	X
X	11	14	X
GND	12	13	X

U5

UPFH	1	18	VCC
0AFA	2	17	52F8
5H21	3	16	HC89
7F7F	4	15	2H70
UUUU	5	14	X
5555	6	13	X
CCCC	7	12	X
84AF	8	11	X
GND	9	10	0001

U6

UPFH	1	18	VCC
0AFA	2	17	52F8
5H21	3	16	HC89
7F7F	4	15	2H70
UUUU	5	14	X
5555	6	13	X
CCCC	7	12	X
84AF	8	11	X
GND	9	10	0001

U7

1293	1	16	VCC
HAP7	2	15	3PCF
3C96	3	14	84AF
3827	4	13	960F
755P	5	12	4154
0001-B	6	11	UA87
1920	7	10	597C
GND	8	9	C34C

U8

0001	1	16	VCC
0000	2	15	F770
0001	3	14	F771
GND	4	13	CCCC
UUUU	5	12	5555
8HUC	6	11	U6AH
8HUA	7	10	U6AF
GND	8	9	960F

X = Don't Care Signature B = Blinking GND or VCC Signature

Table 7-3. Freerun Address Test (Continued)

U9

Signal	Pin	Pin	Signal
0001	1	14	VCC
0001	2	13	HC89
0000	3	12	2H70
0001	4	11	1883
0000-B	5	10	1883
0001-B	6	9	0000-B
GND	7	8	0001-B

U10

Signal	Pin	Pin	Signal
0001-B	1	14	VCC
VCC	2	13	U6AF
0000	3	12	VCC
71U6	4	11	5555
2F8U	5	10	VCC
2F8P	6	9	71U6
GND	7	8	71U7

U11

Signal	Pin	Pin	Signal
84AF	1	14	VCC
0000-B	2	13	0001
84AF	3	12	F771
8HUC	4	11	0001
0001-B	5	10	0000-B
0001-B	6	9	4154
GND	7	8	4154

U12

Signal	Pin	Pin	Signal
0001-B	1	14	VCC
0000-B	2	13	0001
0000-B	3	12	0000
0001-B	4	11	0000
0001	5	10	0001
0000	6	9	0001
GND	7	8	0000

U13

Signal	Pin	Pin	Signal
0000-B	1	20	VCC
0001	2	19	UA87
X	3	18	0001
0001	4	17	X
X	5	16	0001
0001	6	15	X
X	7	14	0001
0001	8	13	X
X	9	12	0001
GND	10	11	X

U14

Signal	Pin	Pin	Signal
GND	1	20	VCC
X	2	19	GND
X	3	18	X
X	4	17	X
X	5	16	X
X	6	15	X
X	7	14	X
X	8	13	X
X	9	12	X
GND	10	11	X

U15

Signal	Pin	Pin	Signal
VCC	1	20	VCC
0001	2	19	0001
X	3	18	X
X	4	17	X
0001	5	16	0001
0001	6	15	0001
X	7	14	X
X	8	13	X
0001	9	12	0001
GND	10	11	C34C

U16

Signal	Pin	Pin	Signal
VCC	1	20	VCC
0001	2	19	0001
X	3	18	X
X	4	17	X
0001	5	16	0001
0001	6	15	0001
X	7	14	X
X	8	13	X
0001	9	12	0001
GND	10	11	1920

U17

Signal	Pin	Pin	Signal
VCC	1	20	VCC
0001	2	19	0001
X	3	18	X
X	4	17	X
0001	5	16	0001
0001	6	15	0001
X	7	14	X
X	8	13	X
0001	9	12	0001
GND	10	11	597C

U18

Signal	Pin	Pin	Signal
0000	1	20	VCC
0001	2	19	4154
0001	3	18	0001
0001-B	4	17	X
0000-B	5	16	0001
0000 or 0001	6	15	X
0000 or 0001	7	14	0001
0000 or 0001	8	13	X
0000 or 0001	9	12	0001
GND	10	11	X

U19

Signal	Pin	Pin	Signal
0001	1	18	VCC
0001	2	17	X
0001	3	16	X
0001	4	15	X
0001	5	14	X
0001	6	13	X
0001	7	12	X
0001	8	11	X
X	9	10	X

U20

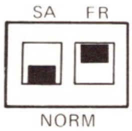
Signal	Pin	Pin	Signal
X	1	14	0001
X	2	13	X
0001	3	12	0001
GND	4	11	VCC
0001	5	10	0001
X	6	9	X
X	7	8	0001

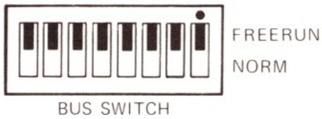
Table 7-4. Freerun ROM Test

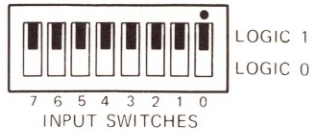
5004A SWITCHES	5036A CONNECTIONS
START	ROM
STOP	ROM
CLOCK	READ

VCC SIGNATURE: 7A70

5036A SWITCHES







SIGNATURES

Data Lines		Address Lines			
D0	A66U	A0	H62U	A8	9635
D1	H278	A1	C21A	A9	1734
D2	1P32	A2	HA07	A10	8P54
D3	14FH	A3	H0AA	A11	0000-B
D4	A314	A4	P030	A12	0000-B
D5	0HF1	A5	4442	A13	0000-B
D6	1HHA	A6	4U2A	A14	0000-B
D7	AC52	A7	0772	A15	0000-B

U1

Signature	Pin	Pin	Signature
GND	1	20	VCC
0000-B	2	19	0000
0000-B	3	18	0000-B
8P54	4	17	0000-B
8P54	5	16	0000-B
1734	6	15	0000-B
1734	7	14	0000-B
9635	8	13	0000-B
9635	9	12	0000-B
GND	10	11	0000-B

U2

Signature	Pin	Pin	Signature
0000	1	20	VCC
H62U	2	19	0772
7A70-B	3	18	0000-B
7A70-B	4	17	7A70-B
C21A	5	16	4U2A
HA07	6	15	4442
7A70-B	7	14	7A70-B
7A70-B	8	13	7A70-B
H0AA	9	12	P030
GND	10	11	7A70-B

U3

Signature	Pin	Pin	Signature
X	1	40	VCC
X	2	39	0000
0000	3	38	0000
0000 or 0001	4	37	7A70-B
0000	5	36	7A70
0000	6	35	7A70
0000	7	34	0000
0000	8	33	7A70
0000	9	32	7A70-B
0000	10	31	7A70
7A70	11	30	0000-B
7A70-B	12	29	7A70
7A70-B	13	28	0000-B
7A70-B	14	27	0000-B
7A70-B	15	26	0000-B
7A70-B	16	25	0000-B
7A70-B	17	24	0000-B
7A70-B	18	23	8P54
0000-B	19	22	1734
GND	20	21	9635

U4

Signature	Pin	Pin	Signature
0772	1	24	VCC
4U2A	2	23	9635
4442	3	22	1734
P030	4	21	7A70
H0AA	5	20	0000-B
HA07	6	19	8P54
C21A	7	18	0000-B
H62U	8	17	AC52
A66U	9	16	1HHA
H278	10	15	0HF1
1P32	11	14	A314
GND	12	13	14FH

U5

Signature	Pin	Pin	Signature
4U2A	1	18	VCC
4442	2	17	0772
P030	3	16	9635
H0AA	4	15	1734
H62U	5	14	A66U
C21A	6	13	H278
HA07	7	12	1P32
7A70-B	8	11	14FH
GND	9	10	7A70

U6

Signature	Pin	Pin	Signature
4U2A	1	18	VCC
4442	2	17	0772
P030	3	16	9635
H0AA	4	15	1734
H62U	5	14	A314
C21A	6	13	0HF1
HA07	7	12	1HHA
7A70-B	8	11	AC52
GND	9	10	7A70

U7

Signature	Pin	Pin	Signature
0000-B	1	16	VCC
0000-B	2	15	0000-B
0000-B	3	14	7A70-B
0000-B	4	13	7A70-B
0000-B	5	12	7A70-B
7A70-B	6	11	7A70-B
7A70-B	7	10	7A70-B
GND	8	9	7A70-B

U8

Signature	Pin	Pin	Signature
7A70	1	16	VCC
0000	2	15	7A70-B
7A70	3	14	0000-B
GND	4	13	HA07
H62U	5	12	C21A
0000-B	6	11	0000-B
7A70-B	7	10	7A70-B
GND	8	9	7A70-B

X = Don't Care Signature B = Blinking GND or VCC Signature

Table 7-4. Freerun ROM Test (Continued)

U9

7A70	1	14	VCC
7A70	2	13	9635
0000	3	12	1734
7A70	4	11	P5AP
0000-B	5	10	P5AP
7A70-B	6	9	0000-B
GND	7	8	7A70-B

U10

7A70-B	1	14	VCC
VCC	2	13	7A70-B
0000	3	12	VCC
7A70-B	4	11	C21A
0000-B	5	10	VCC
7A70-B	6	9	7A70-B
GND	7	8	0000-B

U11

7A70-B	1	14	VCC
0000-B	2	13	7A70
7A70-B	3	12	0000-B
0000-B	4	11	7A70
7A70-B	5	10	0000-B
7A70-B	6	9	7A70-B
GND	7	8	7A70-B

U12

7A70-B	1	14	VCC
0000-B	2	13	7A70
0000-B	3	12	0000
7A70-B	4	11	0000
7A70	5	10	7A70
0000	6	9	7A70
GND	7	8	0000

U13

0000-B	1	20	VCC
7A70	2	19	7A70-B
A66U	3	18	7A70
7A70	4	17	AC52
H278	5	16	7A70
7A70	6	15	1HHA
1P32	7	14	7A70
7A70	8	13	0HF1
14FH	9	12	7A70
GND	10	11	A314

U14

GND	1	20	VCC
A66U	2	19	GND
A66U	3	18	AC52
H278	4	17	AC52
H278	5	16	1HHA
1P32	6	15	1HHA
1P32	7	14	0HF1
14FH	8	13	0HF1
14FH	9	12	A314
GND	10	11	A314

U15

VCC	1	20	VCC
7A70	2	19	7A70
A66U	3	18	AC52
H278	4	17	1HHA
7A70	5	16	7A70
7A70	6	15	7A70
1P32	7	14	0HF1
14FH	8	13	A314
7A70	9	12	7A70
GND	10	11	7A70-B

U16

VCC	1	20	VCC
7A70	2	19	7A70
A66U	3	18	AC52
H278	4	17	1HHA
7A70	5	16	7A70
7A70	6	15	7A70
1P32	7	14	0HF1
14FH	8	13	A314
7A70	9	12	7A70
GND	10	11	7A70-B

U17

VCC	1	20	VCC
7A70	2	19	7A70
A66U	3	18	AC52
H278	4	17	1HHA
7A70	5	16	7A70
7A70	6	15	7A70
1P32	7	14	0HF1
14FH	8	13	A314
7A70	9	12	7A70
GND	10	11	7A70-B

U18

0000	1	20	VCC
7A70	2	19	7A70-B
7A70	3	18	7A70
7A70-B	4	17	14FH
0000-B	5	16	7A70
0000 or 0001	6	15	1P32
0000 or 0001	7	14	7A70
0000 or 0001	8	13	H278
0000 or 0001	9	12	7A70
GND	10	11	A66U

U19

7A70	1	18	VCC
7A70	2	17	X
7A70	3	16	X
7A70	4	15	X
7A70	5	14	X
7A70	6	13	X
7A70	7	12	X
7A70	8	11	X
X	9	10	X

U20

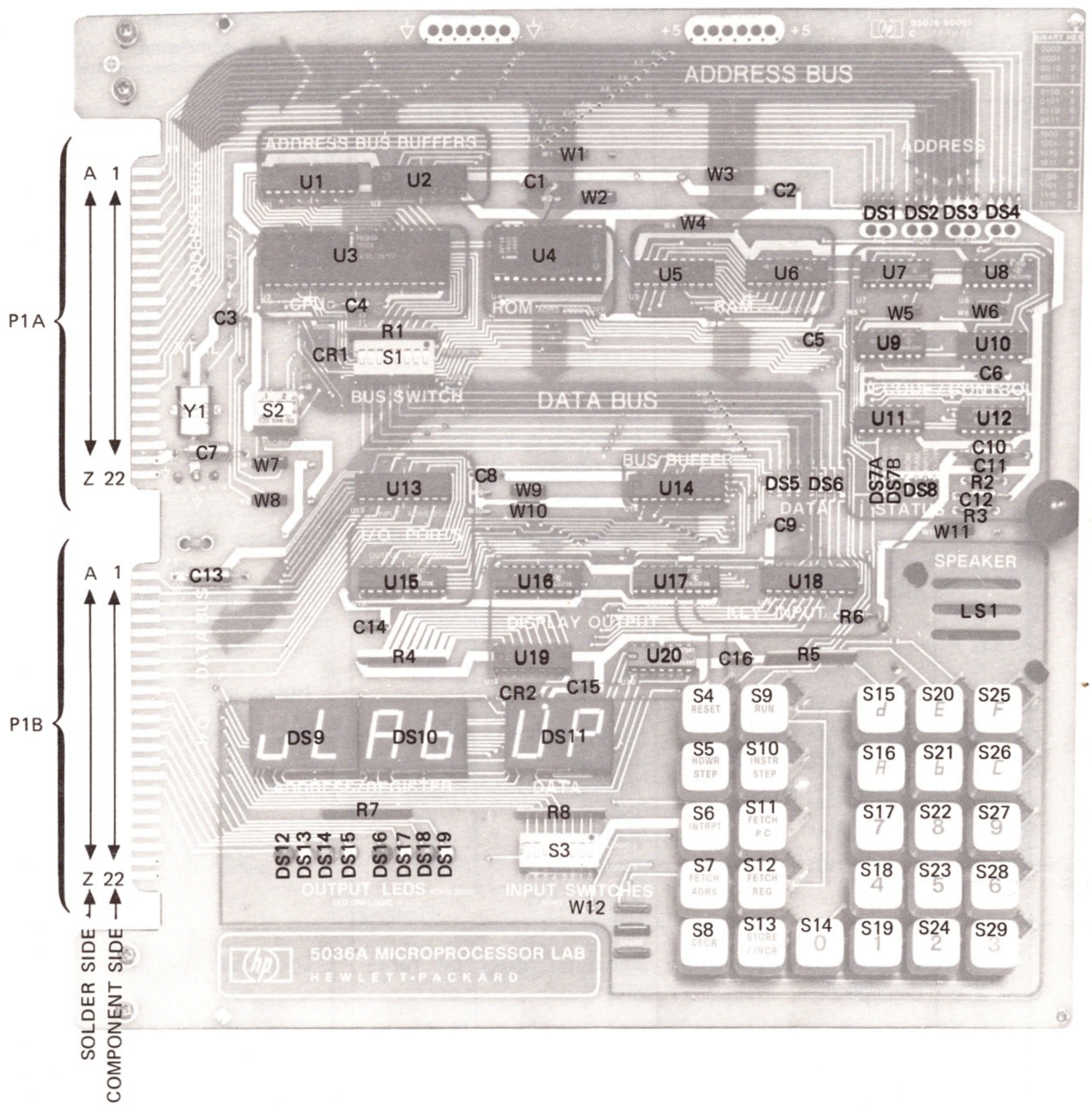
X	1	14	7A70
X	2	13	X
7A70	3	12	7A70
GND	4	11	VCC
7A70	5	10	7A70
X	6	9	X
X	7	8	7A70

7-71. ABBREVIATED TROUBLESHOOTING

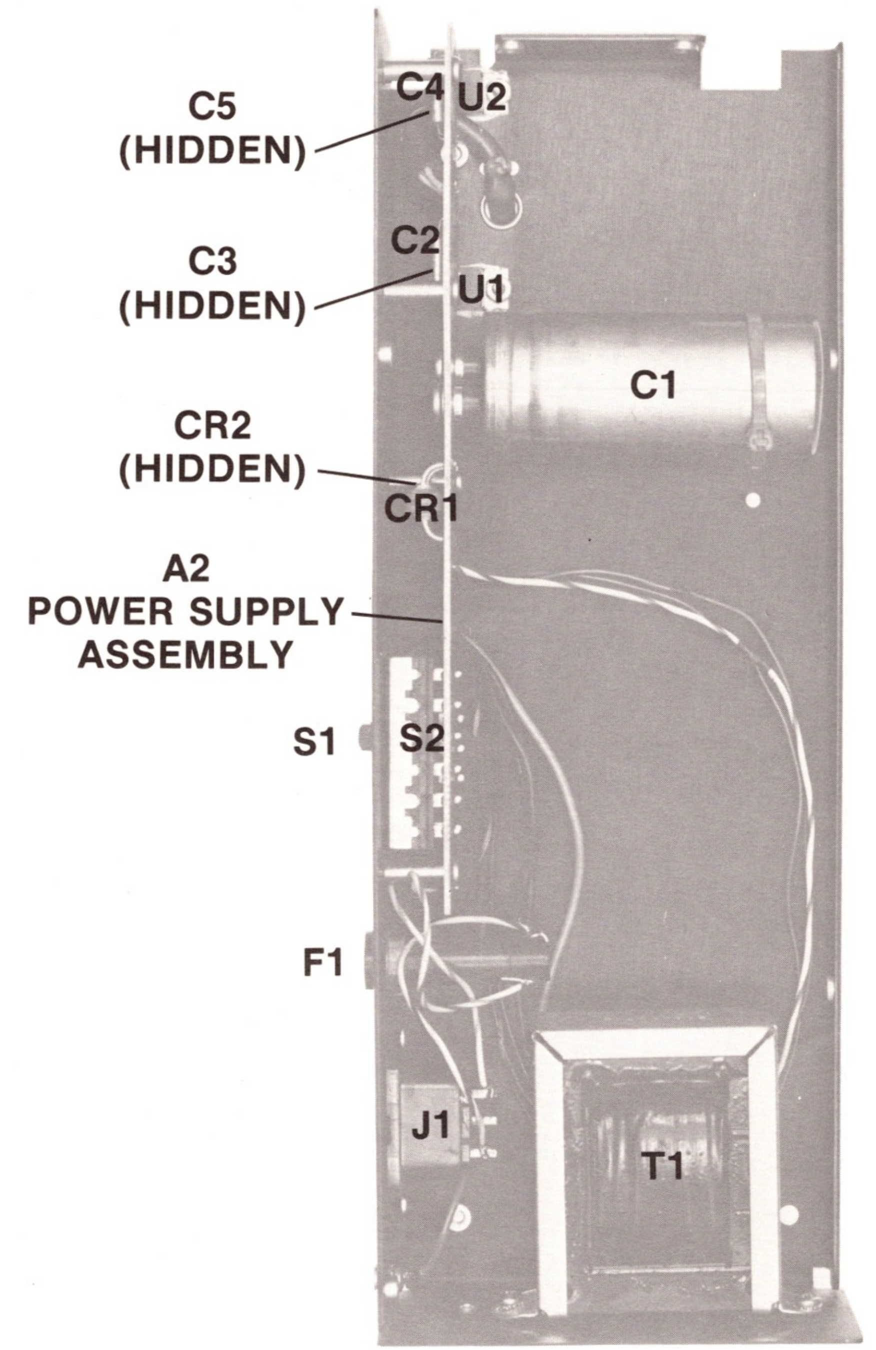
7-72. After becoming familiar with the overall troubleshooting procedures described in detail under paragraph 7-31, use the abbreviated procedures in *Table 7-5.* To use this table, perform each step in the order listed. If a normal indication is received, proceed to the next step. If an abnormal indication is received, perform the procedure in the last column of the table. After a trouble is isolated and corrected, return to step 1 of the table and repeat the procedures.

Table 7-5. Abbreviated Troubleshooting

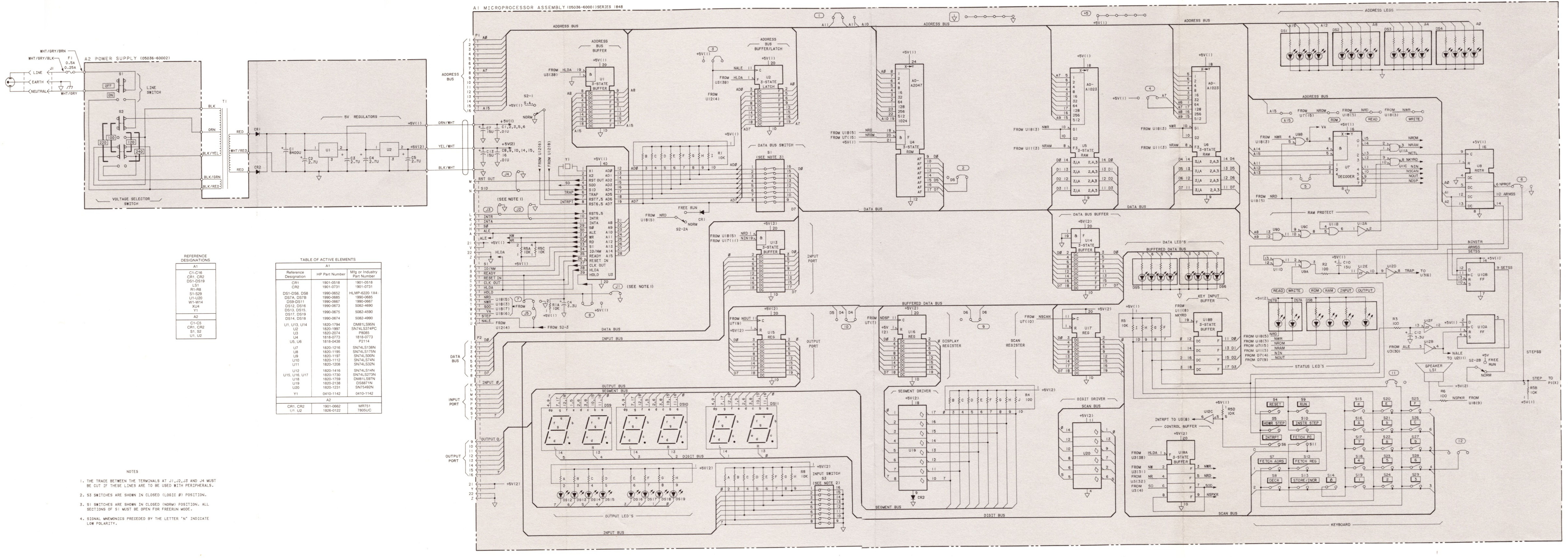
Step	Procedure	Normal Indication	If Indication Is Abnormal
1	Apply power and observe display.	Display indicates uLAb UP	Go to step 2.
2	Observe bus and status LEDs.	Some of the bus and status LEDs are on.	Check Power Supply.
3	Check for bus activity using Logic Probe.	Bus active (changing state or signal activity).	Check U3 pins: Reset — 36 High Hold — 39 Low Clock — 37 Flashing Ready — 35 High
4	Start SA Test Loop: Press RESET. Slide SA switch up and down once.	Output LEDs and display segments light and speaker beeps once. V_{CC} signature as *per Table 7-1 (Write)* or *Table 7-2 (Read).*	Proceed to step 6 for Freerun Test.
5	Take signatures per paragraph 7-52 (Write) or 7-54 (Read).	Signatures correct per *Table 7-1* or *Table 7-2*	1. Locate bad signature. 2. Trace signal path back until correct signature is found. 3. Isolate fault.
6	Start Freerun Test: Slide 8 BUS SWITCHES up. Slide FR switch up.	A0 through A13 address bus LEDs lit. A14 and A15 LEDs flashing. Status LEDs as follows: READ — On WRITE — Off ROM, RAM INPUT, OUTPUT Flashing	Check control lines (Step 3) and clock. Check data bus pins of U3.
7	Take signatures per paragraph 7-68.	Signatures correct per *Table 7-3.*	1. Locate bad signature. 2. Trace signal path back until correct signature is found. 3. Isolate fault.
8	Take signatures per paragraph 7-70.	Signatures correct per *Table 7-4.*	If one data bus signature is bad, check corresponding ROM output pin. If all data bus lines bad, check ROM enable and address pins. If good, check all bus device enable pins.



P/O Figure 7-5. A1 Microprocessor Assembly



P/O Figure 7-5. A2 Power Supply



REFERENCE DESIGNATIONS

A1
C1-C16 CR1, CR2 DS1-DS19 LS1 R1-R8 S1-S29 U1-U20 W1-W14 XU4 Y1
A2
C1-C5 CR1, CR2 S1, S2 U1, U2

TABLE OF ACTIVE ELEMENTS

Reference Designation	HP Part Number	Mfg or Industry Part Number
A1		
CR1	1901-0518	1901-0518
CR2	1901-0731	1901-0731
DS1-DS6, DS8	1990-0652	HLMP-6220(1X4)
DS7A, DS7B	1990-0685	1990-0685
DS9-DS11	1990-0667	1990-0667
DS12, DS16	1990-0673	5082-4690
DS13, DS15, DS17, DS19	1990-0675	5082-4590
DS14, DS18	1990-0674	5082-4990
U1, U13, U14	1820-1794	DM81LS95N
U2	1820-1997	SN74LS374PC
U3	1820-2074	P8085
U4	1818-0773	1818-0773
U5, U6	1818-0438	P2114
U7	1820-1216	SN74LS138N
U8	1820-1195	SN74LS175N
U9	1820-1197	SN74LS00N
U10	1820-1112	SN74LS74N
U11	1820-1208	SN74LS32N
U12	1820-1416	SN74LS14N
U15, U16, U17	1820-1730	SN74LS273N
U18	1820-1759	DM81LS97N
U19	1820-2138	DS8871N
U20	1820-1231	SN75492N
Y1	0410-1142	0410-1142
A2		
CR1, CR2	1901-0662	MR751
U1, U2	1826-0122	7805UC

NOTES

1. THE TRACE BETWEEN THE TERMINALS AT J1,J2,J3 AND J4 MUST BE CUT IF THESE LINES ARE TO BE USED WITH PERIPHERALS.
2. S3 SWITCHES ARE SHOWN IN CLOSED (LOGIC Ø) POSITION.
3. S1 SWITCHES ARE SHOWN IN CLOSED (NORM) POSITION. ALL SECTIONS OF S1 MUST BE OPEN FOR FREERUN MODE.
4. SIGNAL MNEMONICS PRECEDED BY THE LETTER 'N' INDICATE LOW POLARITY.

Figure 7-5. 5036A Schematic Diagram

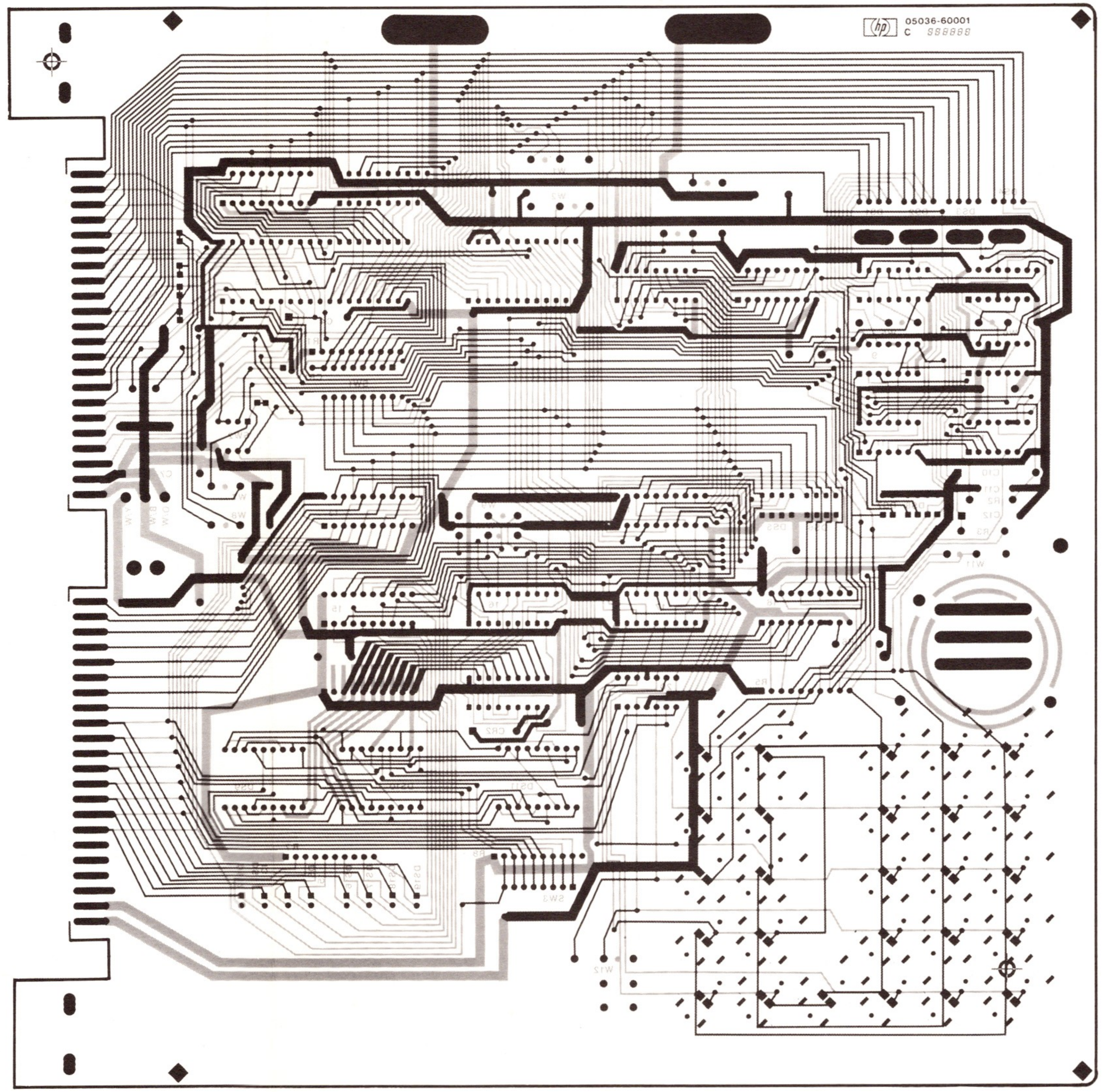


Figure 7-6. *Signal Tracing Diagram*

SALES & SUPPORT OFFICES
Arranged Alphabetically by Country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

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MANUAL PART NO. 05036-90001

PRINTED IN U.S.A.

MANUAL CHANGES

CHANGE DATE: April 13, 1982
This change supersedes all earlier dated changes.

*** Make all corrections listed under ERRATA before making other changes.

*** Check following table for your instrument's serial prefix or series number and make listed change(s) to manual.

MANUAL DESCRIPTION

INSTRUMENT:	5036A Microprocessor Lab Service Manual
SERIAL PREFIX:	1848A
DATE PRINTED:	FEB 1979
HP PART NO:	05036-90001
MICROFICHE NO:	05036-90002

# INDICATES NEW OR REVISED ITEM

> INDICATES ACTION TO BE TAKEN

SERIAL PREFIX OR SERIES NUMBER	MANUAL CHANGE(S)	SERIAL PREFIX OR SERIES NUMBER	MANUAL CHANGE(S)
1936A	1		
2112A	1,2		
2116A	1,2,3		
#2212A	1,2,3,4		

Information for any optional circuit boards described in this manual agrees with the series numbers on the circuit board(s) for the option, which may not be the same as the Serial Prefix Number on the rear of the instrument.

(C5036ASX) 1=8957/2=11247/3=11260/4=12795

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ERRATA

Front Inside Cover:
>Change "1848" to 1848A.

Page 5-5, Table 5-1, Replaceable Parts:
>Add "SERIES 1848" to A1 description.

Page 5-6, Table 5-1. Chassis Parts. Replaceable Parts:
>Add 05036-4001, Qty 2, Board Assembly Hinge.
>Change STRAP,SETUP HP PART Number to 9223-0472.

Page 7-25, Figure 7-5, Schematic Diagram:
>Add "P/O P1" over terminal M on left edge of schematic.
>Change source of "VA" output at terminal "V" to U9(6) in place of U18(6).
>Change source of "NIN" input at U13 pin 19 to U7(11) in place of U17(11).

CHANGE 1

Page 5-5, Table 5-1. Replaceable Parts:
>Change A1 Series Number to 1936.
>Add A1XU3; 1200-0616; CD=1; SOCKET-IC 40-CONTACTS; 28480; 1200-0616.

Page 7-25, Figure 7-5. A1 Schematic Diagram:
>Change A1 Series Number (top of diagram) to 1936.

CHANGE 2

Page 5-5, Table 5-1. Replaceable Parts:
>Change A1 Microprocessor Assembly Series Number to 2112.
>Change A1DS9, DS10, and DS11 to 1990-0807; DISPLAY 7SEG DUL.

Page 5-6, Table 5-1. Replaceable Chassis Parts:
>Change F1 (2110-0004) to 2110-0018; FUSE .25A 250V SLO-BLO TD 1.25X.25UL.

Page 7-25, Figure 7-5. 5036A Schematic Diagram:
>Change A1 Microprocessor Assembly Series Number to 2112.
>Change Part Numbers for DS9-DS11 to 1990-0807 in TABLE OF ACTIVE ELEMENTS.

CHANGE 3

Page 5-5, Table 5-1. A1 (05036-60001) Replaceable Parts:
>Change A1 Microprocessor Assembly Series Number to 2116.
>Add A1XDS9, A1XDS10 and A1XDS11; 1200-0949; SOCKET-18 PIN DIP

Page 7-25, Figure 7-5. 5036A Schematic Diagram:
>Change A1 Microprocessor Assembly Series Number to 2116.

#CHANGE 4

Page 5-6, Table5-1. CHASSIS PARTS. Replaceable Parts:
>Delete 1540-0537, no description.
>Add 1540-0781, Qty 1, CASE-CARRYING.
>Add 2360-0115, Qty 4, SCREW-MACHINE 6-32 .312-IN-LG PAN-HD-POZI.